

80 Segment / 16 Common Controller  
for Dot Matrix LCD

## FEATURES

### Internal Memory

- Character Generator ROM (CGROM) : 7840bits  
(224 characters × 5 × 7dot)
- Character Generator RAM (CGRAM) : 160 bit (4-  
characters × 5 × 8 dot)
- Display Data RAM (DDRAM) : 256bits (32  
characters × 8bits)
- Low power operation
  - Power supply voltage range : 2.7 ~ 5.5V ( $V_{DD}$ )
  - LCD drive voltage range : 3.0 ~ 7.0 ( $V_{DD}-V_5$ )
- CMOS process
- Duty cycle : 1/16
- Built-in oscillator
- Low power consumption
- Internal divide resistor for LCD driving voltage
- Available for COG

## DOT MATRIX LCD CONTROL- LER & DRIVER

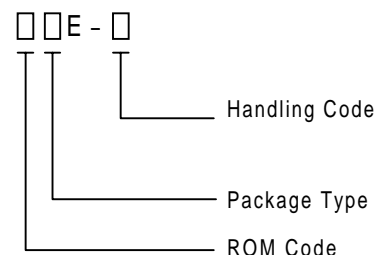
APU0071 is a dot matrix LCD driver & controller LSI that is fabricated by low power CMOS technology. It is capable of displaying 1-line 16 characters or 2 line 16 characters with 5 × 8 dots format.

## FUNCTIONS

Character type dot matrix LCD driver & controller.

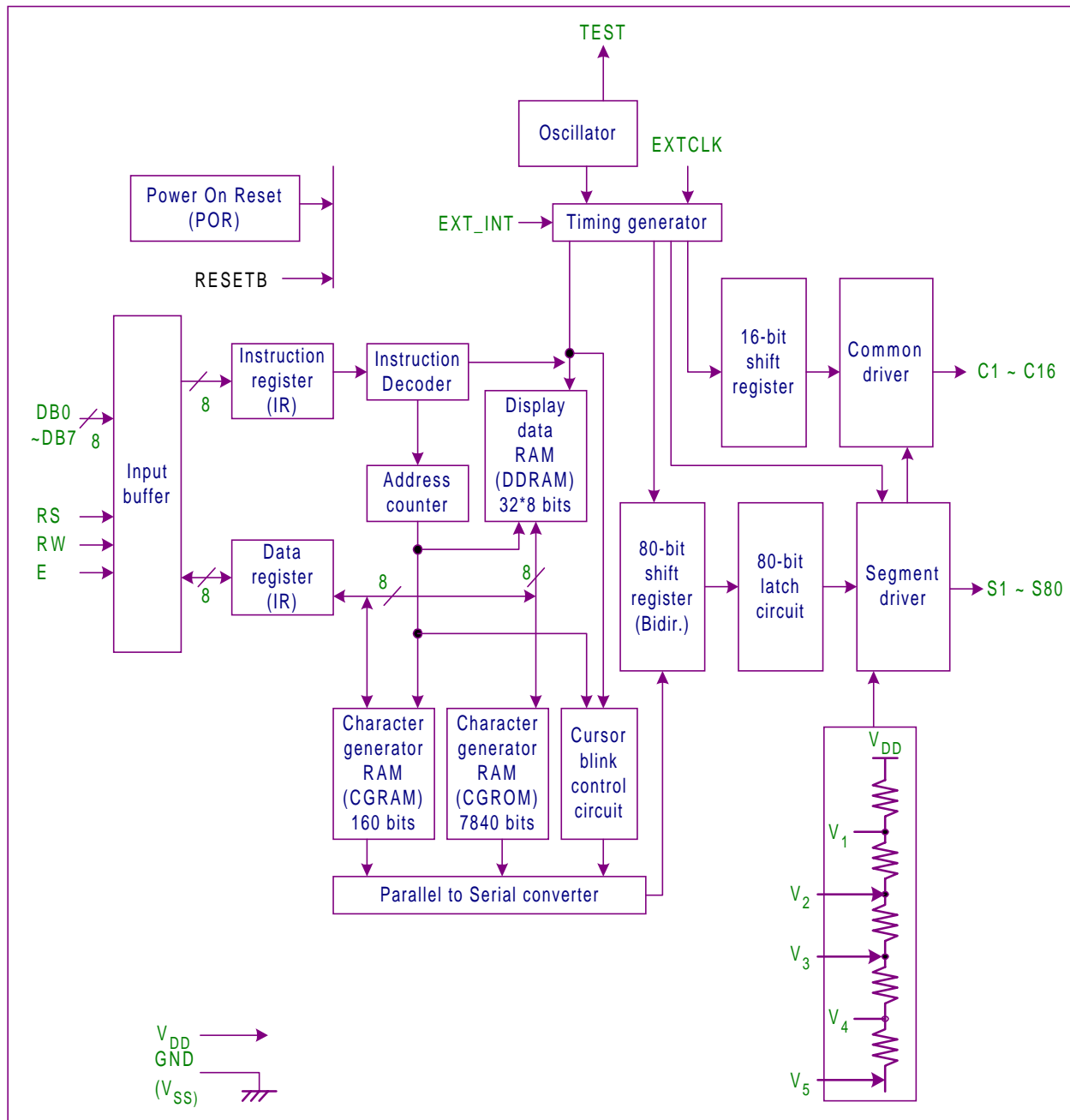
- Easy interface with 4-bit or 8-bit MPU.
- Internal driver : 16 common and 80 segment signal output.
- Display character pattern : 5 × 7 dots format (224 kinds)
- Direct programming of the special character patterns by character Generator RAM.
- Mask open for programming customer character patterns
- Various instructions function.
- Automatic power on reset.

## ORDERING INFORMATION

<p style="margin-left: 20px;">APU0071 □□E - □</p>  <p style="margin-left: 100px;">Handling Code</p> <p style="margin-left: 100px;">Package Type</p> <p style="margin-left: 100px;">ROM Code</p>	<p>ROM Code 001 : Standard 002 : Customer</p> <p>Package Type W : COG</p> <p>Handling Code TY : Tray</p>
--	--

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

**BLOCK DIAGRAM**

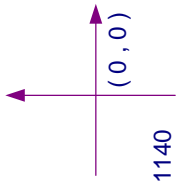


## PAD DIAGRAM

**APU0071  
PAD Diagram**

S01	39
S02	40
S03	41
S04	42
S05	43
S06	44
S07	45
S08	46
S09	47
S10	48
S11	49
S12	50
S13	51
S14	52
S15	53
S16	54
S17	55
S18	56
S19	57
S20	58
S21	59
S22	60
S23	61
S24	62
S25	63
S26	64
S27	65
S28	66
S29	67
S30	68
S31	69
S32	70
S33	71
S34	72
S35	73
S36	74
S37	75
S38	76
S39	77
S40	78
S41	79
S42	80
S43	81
S44	82
S45	83
S46	84
S47	85
S48	86
S49	87
S50	88
S51	89
S52	90
S53	91
S54	92
S55	93
S56	94
S57	95
S58	96
S59	97
S60	98
S61	99
S62	100
S63	101
S64	102
S65	103
S66	104
S67	105
S68	106
S69	107
S70	108
S71	109
S72	110
S73	111
S74	112
S75	113
S76	114
S77	115
S78	116
S79	117
S80	118

C8	38
C7	37
C6	36
C5	35
C4	34
C3	33
C2	32
C1	31



Chip size 6500 x 1140

30	DB7
29	DB6
28	DB5
27	DB4
26	DB3
25	DB2
24	DB1
23	DB0
22	E
21	R_NW
20	RS
19	EXT_RST
18	CLK1_TS
17	M_TS
16	V <sub>DD</sub>
15	V <sub>DD</sub>
14	V <sub>DD</sub>
13	V <sub>2</sub>
12	Dummy
11	V <sub>3</sub>
10	V <sub>5</sub>
9	V <sub>5</sub>
8	V <sub>5</sub>
7	V <sub>SS</sub>
6	V <sub>SS</sub>
5	V <sub>SS</sub>
4	EXT_INT
3	EXTCLK
2	OSC_TS
1	POR_TS

119	C16
120	C15
121	C14
122	C13
123	C12
124	C11
125	C10
126	C9

**AP**

PAD NO. : 1 ~ 30  
 PAD PITCH : ≥ 120  
 AL PAD SIZE : 96 × 96  
 AL PAD WINDOW: 70 × 70  
 AU PAD SIZE : 84 × 84  
 UNIT : μm

PAD NO. : 31 ~ 126  
 PAD PITCH : 80  
 AL PAD SIZE : 62 × 102  
 AL PAD WINDOW: 36 × 76  
 AU PAD SIZE : 50 × 90  
 UNIT : μm

## PAD LOCATION

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
1	POR_TS	-2650.9	-429.84	43	S5	2843.35	404.67	85	S47	-516.65	404.67
2	OSC_TS	-2530.9	-429.84	44	S6	2763.35	404.67	86	S48	-596.65	404.67
3	EXTCLK	-2410.9	-429.84	45	S7	2683.35	404.67	87	S49	-676.65	404.67
4	EXT_INT	-2290.9	-429.84	46	S8	2603.35	404.67	88	S50	-756.65	404.67
5	V <sub>SS</sub>	-2158.65	-480.84	47	S9	2523.35	404.67	89	S51	-836.65	404.67
6	V <sub>SS</sub>	-2038.65	-480.84	48	S10	2443.35	404.67	90	S52	-916.65	404.67
7	V <sub>SS</sub>	-1918.65	-480.84	49	S11	2363.35	404.67	91	S53	-996.65	404.67
8	V <sub>5</sub>	-1728.70	-480.84	50	S12	2283.35	404.67	92	S54	-1076.65	404.67
9	V <sub>5</sub>	-1608.70	-480.84	51	S13	2203.35	404.67	93	S55	-1156.65	404.67
10	V <sub>5</sub>	-1488.70	-480.84	52	S14	2123.35	404.67	94	S56	-1236.65	404.67
11	V <sub>3</sub>	-1305.75	-480.84	53	S15	2043.35	404.67	95	S57	-1316.65	404.67
12	DUMMY	-1119.15	-480.84	54	S16	1963.35	404.67	96	S58	-1396.65	404.67
13	V <sub>2</sub>	-940.20	-480.84	55	S17	1883.35	404.67	97	S59	-1476.65	404.67
14	V <sub>DD</sub>	-749.60	-480.84	56	S18	1803.35	404.67	98	S60	-1556.65	404.67
15	V <sub>DD</sub>	-629.60	-480.84	57	S19	1723.35	404.67	99	S61	-1636.65	404.67
16	V <sub>DD</sub>	-509.60	-480.84	58	S20	1643.35	404.67	100	S62	-1716.65	404.67
17	M_TS	-333.50	-480.84	59	S21	1563.35	404.67	101	S63	-1796.65	404.67
18	CLK1_TS	-102.10	-480.84	60	S22	1483.35	404.67	102	S64	-1876.65	404.67
19	EXT_RST	131.70	-480.84	61	S23	1403.35	404.67	103	S65	-1956.65	404.67
20	RS	358.80	-480.84	62	S24	1323.35	404.67	104	S66	-2036.65	404.67
21	R_NW	594.20	-480.84	63	S25	1243.35	404.67	105	S67	-2116.65	404.67
22	E	821.30	-480.84	64	S26	1163.35	404.67	106	S68	-2196.65	404.67
23	DB0	1054.80	-480.84	65	S27	1083.35	404.67	107	S69	-2276.65	404.67
24	DB1	1286.80	-480.84	66	S28	1003.35	404.67	108	S70	-2356.65	404.67
25	DB2	1518.40	-480.84	67	S29	923.35	404.67	109	S71	-2436.65	404.67
26	DB3	1750.40	-480.84	68	S30	843.35	404.67	110	S72	-2516.65	404.67
27	DB4	1982.00	-480.84	69	S31	763.35	404.67	111	S73	-2596.65	404.67
28	DB5	2214.00	-480.84	70	S32	683.35	404.67	112	S74	-2676.65	404.67
29	DB6	2445.60	-480.84	71	S33	603.35	404.67	113	S75	-2756.65	404.67
30	DB7	2631.91	-429.84	72	S34	523.35	404.67	114	S76	-2836.65	404.67
31	C1	3149.01	-475.85	73	S35	443.35	404.67	115	S77	-2916.65	404.67
32	C2	3149.01	-395.85	74	S36	363.35	404.67	116	S78	-2996.65	404.67
33	C3	3149.01	-315.85	75	S37	283.35	404.67	117	S79	-3076.65	404.67
34	C4	3149.01	-235.85	76	S38	203.35	404.67	118	S80	-3156.65	404.67
35	C5	3149.01	-155.85	77	S39	123.35	404.67	119	C16	-3137.66	95.82
36	C6	3149.01	-75.85	78	S40	43.35	404.67	120	C15	-3137.66	15.82
37	C7	3149.01	4.15.00	79	S41	-36.65	404.67	121	C14	-3137.66	-64.18
38	C8	3149.01	84.15	80	S42	-116.65	404.67	122	C13	-3137.66	-144.18
39	S1	3163.35	404.67	81	S43	-196.65	404.67	123	C12	-3137.66	-224.18
40	S2	3083.35	404.67	82	S44	-276.65	404.67	124	C11	-3137.66	-304.18
41	S3	3003.35	404.67	83	S45	-356.65	404.67	125	C10	-3137.66	-384.18
42	S4	2923.35	404.67	84	S46	-436.65	404.67	126	C9	-3137.66	-464.18

**PIN DESCRIPTION**

PIN	Input / Output	Name	Description	Interface
V <sub>DD</sub>	P	Power supply & LCD Bias pin	For logical circuit (+3v,+5v)	Power Supply
V <sub>SS</sub> (GND)			0V (GND)	
V <sub>2</sub> , V <sub>3</sub> , V <sub>5</sub>			Bias voltage level for LCD driving	
S1 ~ S80	Output	Segment output	Segment signal output for LCD driving	LCD
C1 ~ C16	Output	Common output	Common signal output for LCD driving	LCD
EXTCLK	Input	External clock Input	When using external clock, used as clock input pin. When using internal oscillator, connect to V <sub>DD</sub> or V <sub>SS</sub> .	External clock
EXT_INT	Input	External / Internal oscillator clock select	When EXT_INT = "High", external clock is used. When "Low", instruction oscillator is used.	MPU
RS	Input	Register select	Used as register selection input. When RS = "High", data register is selected. When RS = "Low", instruction register is selected.	MPU
R_NW	Input	Read / Write	Used as read / write selection input. When RW = "High", read operation. When RW = "Low", write operation.	
E	Input	Read / Write enable	Used as read / write enable signal.	
DB0 ~ DB3	Input / Output	Data Bus 0 ~ 7	When 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode open these pins.	
DB4 ~ DB7			When 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 is used for Busy Flag output during read instruction operation.	
EXT_RST	Input	Reset	If it is necessary to initialize the system by hardware, force "Low", level signal to this terminal about 1.2 ms.	
OSC_TS	Output	Test Pin	Internal oscillator test pin. Open this pin.	
POR_TS	Output	Test Pin	Internal test pin. Open this pin.	
M_TS	Output	Test Pin	Internal test pin. Open this pin.	
CLK1_TS	Output	Test Pin	Internal test pin. Open this pin.	

## **FUNCTION DESCRIPTION**

### **1. SYSTEM INTERFACE**

This chip consists of two kinds of interface type with MPU : 4-bit bus and 8-bit bus.  
4-bit bus and 8-bit bus is selected by DL bit of function set in the instruction register.

During read or write operation, two 8-bit registers are used. One is the data register (DR); the other is the instruction register (IR) .

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM / CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

Thus, after MPU reads DR data, the data in the next DDRAM / CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM / CGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU.  
MPU cannot read data from instruction register.

Table 1. Various kinds of operation according to RS and R / W bits.

RS	R / L	Operation
0	0	Instruction Write operation (MPU Writes Instruction into IR)
0	1	Read Busy flag (DB7) and address counter (DB0 ~ DB6)
1	0	Data Write operation (MPU Writes data into DR)
1	1	Data Read operation (MPU Reads data into DR)

The register selection depends on RS input pin setting in both 4-bit bus mode.

### **2. BUSY FLAG (BF)**

BF = "High" it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R / W = High (Read instruction Operation) , through DB7 port.

Before exciting the next instruction, be sure that BF is not High.

### **3. ADDRESS COUNTER (AC)**

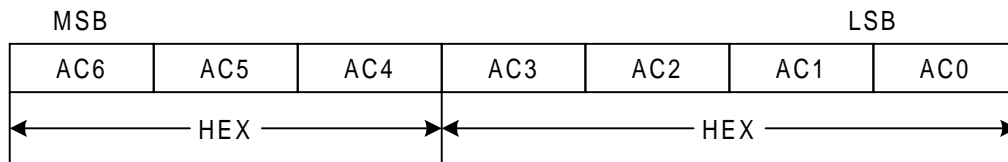
Address Counter (AC) stores the address of DDRAM / CGRAM that are transferred from IR.

After writing into (reading from) DDRAM / CGRAM data, AC is increased (decreased) by 1 automatically.

When RS = "Low", and R / W = "High", AC value can be read through DB0 ~ DB6 ports.

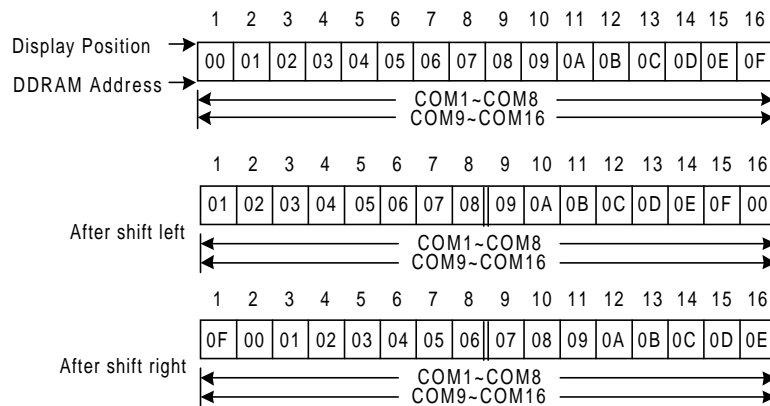
## 4. DISPLAY DATA RAM (DDRAM)

DDRAM stores 8bits character code in CGROM / CGRAM and its maximum number is 32 (32 Characters) . DDRAM address is set by the address counter (AC) as a hexadecimal number.



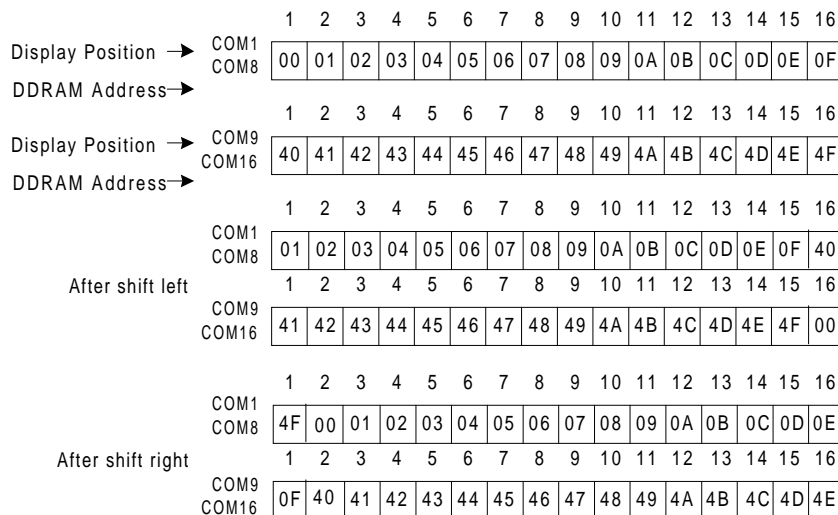
### 4-1. DDRAM addressing mode 0 (A = 0) (1 Line)

In this addressing mode, the address range of DDRAM is 00H ~ 0FH.



### 4-2. DDRAM addressing mode 1 (A = 1) (2 Line)

In this addressing mode, the address range of DDRAM is 00H ~ 0FH and 40H ~ 4FH.



### 5. CHARACTER GENERATOR RAM (CGRAM)

CGRAM is used for user defined character pattern. The format of the character pattern is  $5 \times 7$  dots except for the cursor position and has a maximum of 4 characters. To use the character pattern in CGRAM write the character code into DDRAM as shown in table 2.

Table 2. Relationship between character Code (DDRAM) and Character Pattern (CGRAM)

Character Code ( DDRAM data )								CGRAM address					CGRAM data					Pattern Number
7	6	5	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0	
0	0	0	0	*	*	0	0	0	0	0	0	0	0	1	1	1	0	Pattern 1
								0	0	0	0	1	1	0	0	0	1	
								0	0	0	1	0	1	0	0	0	1	
								0	0	0	1	1	1	1	1	1	1	
								0	0	1	0	0	1	0	0	0	1	
								0	0	1	0	1	1	0	0	0	1	
								0	0	1	1	0	1	0	0	0	1	
								0	0	1	1	1	0	0	0	0	0	
				⋮				⋮		⋮			⋮		⋮			⋮
0	0	0	0	*	*	0	0	1	1	0	0	0	1	1	1	1	0	Pattern 4
								1	1	0	0	1	1	0	0	0	1	
								1	1	0	1	0	1	0	0	0	1	
								1	1	0	1	1	1	0	0	0	1	
								1	1	1	0	0	1	0	0	0	1	
								1	1	1	0	1	1	0	0	0	1	
								1	1	1	1	0	1	1	1	1	0	
								1	1	1	1	1	0	0	0	0	0	

Note : The asterisk means "don't care".



## **6. CHARACTER GENERATOR ROM (CGROM)**

CGROM generates  $5 \times 5 \times 7$  character pattern from character generate code in DDRAM. CGROM has  $5 \times 7$ -dot 224-character pattern excluding cursor position. The relationship between character code and character pattern can be referred to Table 5.

## **7. TIMING GENERATION CIRCUIT**

Timing generation circuit generates clock signals for the internal operations.

## **8. LCD DRIVER CIRCUIT**

LCD driver circuit has 16 common and 80 segment output signals for LCD driving. Data from CGRAM / CGROM is transferred to 80-bit segment shift register in a serially, which is then it is stored to 80-bit segment output latch. When each COM is selected by a 16-bit common register, the segment data also outputs through segment driver from 40-bit segment output latch.

## **9. CURSOR / BLINK CONTROL CIRCUIT**

It controls cursor / blink ON / OFF at the cursor position.

# **INSTRUCTION DESCRIPTION**

## **1. OUTLINE**

To overcome the speed difference between the internal clock of APU0071 and the MPU clock, the APU0071 performs an internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read / write and data bytes.

Instruction can be divided into four types :

- 1-1. APU0071 function set instructions (set display methods, set data length, etc.)
- 1-2. Address set instructions to internal RAM
- 1-3. Data transfer instructions with internal RAM
- 1-4. Others

The address of internal RAM is automatically increased or increased by 1.

Note : During an internal operation, the Busy Flag (DB7) is High. Busy Flag check must precede the next instruction.

Table 3. Instruction Table

Instruction	Instruction Code										Description	Execution time (f <sub>osc</sub> =270 kHz)	
	RS	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.	629μs	
Return Home	0	0	0	0	0	0	0	0	0	1	* Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	629μs	
Entry Mode Set	0	0	0	0	0	0	0	0	1	I / D	S Assign cursor moving direction and enable entire display shift.	37μs	
Display ON / OFF Control	0	0	0	0	0	0	0	1	D	C	B All display (D) , cursor (C) , and blinking of cursor position character on / off control bit (B) .	37μs	
Cursor or Display Shift	0	0	0	0	0	0	1	S / C	R / L	*	* Cursor and Display shift and their direction control without changing DDRAM data.	37μs	
Function Set	0	0	0	0	0	1	DL	A	*	M1	M0 Set interface data length (DL) , DDRAM addressing mode (A) and COM / SEG output pattern (M0, M1) .	37μs	
Set CGRAM Address	0	0	0	1	*	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	37μs	
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	37μs	
Read Busy Flag and Address	DDRAM	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether in internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
	CGRAM				*	*	AC4	AC3	AC2	AC1	AC0		
Write Data to RAM	DDRAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM) .	43μs
	CGRAM			*	*	*	D4	D3	D2	D1	D0		
Read Data from RAM	DDRAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM) .	43μs
	CGRAM			*	*	*	D4	D3	D2	D1	D0		

I / D = 1 : Increment,

S = 1 : Shift enable,

S / C = 1 : Display shift,

R / L = 1 : Shift right,

D / L = 1 : 8 bit interface,

A = 0 : DDRAM addressing mode 0,

M0 = 0 : Bottom view,

M1 = 0 : No Rotate,

BF = 1 : System is in operation

I / D = 0 : Decrement

S = 0 : Shift disable

S / C = 0 : Move cursor

R / L = 0 : Shift left

D / L = 0 : 4-bit interface

A = 1 : DDRAM addressing mode1

M0 = 1 : Top view

M1 = 1 : Rotate

BF = 0 : System is ready

## 1-1. Clear Display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code of CGROM) to all DDRAM address, and set DDRAM address to "00H" into AC (Address Counter) . For this instruction, the CGROM address "20H" has to be set to space code. Shifting of the display position returns it to the original position. Namely, when display data is disappeared and cursor or blinking is displayed, bring the cursor to the left edge on first line of the display. It makes entry mode to increment (I / D = 1)

## 1-2. Return Home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	*

"\*" : Don't care

Set DDRAM address to "00H" into the address counter. Shifting of the display position returns it to the original position. When cursor or blinking is displayed, bring the cursor to the left edge on first line of the display. The data in DDRAM does not change.

## 1-3. Entry Mode Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I / D	S

Set the moving direction of cursor and display.

I / D : Increment / decrement of DDRAM / CGRAM address (cursor or blink)

When I / D = "High", cursor / blink moves to right and DDRAM address is increased by 1.

When I / D = "Low", cursor / blink moves to left and DDRAM address is decreased by 1.

S : Shift of entire display

When DDRAM read (CGRAM read / write) operation or S = "Low", entire display is not shifting.

If S = "High", and DDRAM write operation, entire display is sifted according to I / D value (I / D = "1" : shift left, I / D = "0" : shift right) .

## 1-4. Display ON / OFF Control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Control display / cursor / blink ON / OFF 1 bit register.

D : Display ON / OFF control bit

When D = "High", entire display is turned on.

When D = "Low", entire display is turned off, but display data is remains in DDRAM.

C : Cursor ON / OFF control bit

When C = "High", cursor is turned on.

When C = "Low", cursor is disappeared in current display, but I / D register preserves its data.

B : Cursor Blink ON / OFF control bit

When B = "High", cursor blink is on, performs alternately between all high data (black pattern) and display character at the cursor position.

When B = "Low", blink is off.

## 1-5. Cursor or Display Shift

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S / C	R / L	*	*

" \* " : Don't care

Without writing or reading of display data, shift right / left the cursor position or display.

This instruction is used to correct or search display data.

During 2-line mode display, cursor moves to the 2nd line after 16th digit of 1st line.

Note that display shift is performed simultaneously in all the line.

When displayed data is shifted repeatedly, each line is shifted individually.

When display shift is performed, the contents of address counter are not changed.

Table 4. Shift patterns according to S / C and R / L bits

S / C	R / L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

## 1-6. Function Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	A	*	M1	M0

" \* " : Don't care

DL : Interface data length control bit

When DL = "High", 8-bit bus mode with MPU.

When DL = "Low", 4-bit bus mode with MPU. Thus, DL is a signal to select 8-bit or 4-bit bus mode.

In 4-bit bus mode, the 4-bit data is transferred twice.

A : Set the display data-addressing mode

When A = "Low", DDRAM addressing mode 0. (1 Line)

When A = "High", DDRAM addressing mode 1. (2 Line)

M0 : Set COM / SEG output rotation

When M0 = "Low", Bottom view.

When M0 = "High", Top view.

M1 : Set display line and character mode

When M1 = "Low", LCD module Rotation mode A.

When M1 = "High", LCD module Rotation mode B.

(Refer to Application information)

## 1-7. Set CGRAM Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	*	AC4	AC3	AC2	AC1	AC0

MSB

LSB

" \* " : Don't care

Set CGRAM address to AC.

This instruction allows the MPU to access CGRAM data for user defined character pattern.

Available CGRAM Address is lower 5 bits (DB4 ~ DB0) .

## 1-8. Set DDRAM Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction allows the MPU to access DDRAM data.

When DDRAM addressing mode 1 (A = 0) , DDRAM address is from "00H" to "0FH".

In DDRAM addressing mode 2 (A = 1) , DDRAM address range of the 1st 16 character is "00H" to "0FH", and DDRAM address range of the 2nd 16 character is "40H" to "4FH".

## 1-9. Read Busy Flag & Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Code	0	0	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	DDRAM	
				MSB								LSB
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Code	0	0	BF	*	*	AC4	AC3	AC2	AC1	AC0	CGRAM	
				MSB							LSB	

" \* " : Don't care

This instruction shows whether APU0071 is in internal operation or not. If the resultant BF is High, The internal operation is in progress and should wait until BF to be Low, which by then the next instruction can be performed. In the instruction you can read also the value of address counter.

## 1-10. Write data to RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0	DDRAM	
				MSB								LSB
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Code	1	0	*	*	*	D4	D3	D2	D1	D0	CGRAM	
				MSB							LSB	

" \* " : Don't care

Write binary 8/5 bit data to DDRAM / CGRAM. The selection of RAM from DDRAM / CGRAM is set by the previous address set instruction (DDRAM address set, CGRAM address set) . After writing operation, the address is automatically increased / decreased by 1, according to the entry mode.

## 1-11. Read data from RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0	DDRAM
	MSB					LSB					
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Code	1	0	*	*	*	D4	D3	D2	D1	D0	CGRAM
	MSB					LSB					

" \* " : Don't care

Read BINARY 8 / 5 bit from DDRAM / CGRAM. The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, data that was read first becomes invalid, as the direction of AC is not determined. If RAM data is read several times without RAM address set instruction before read operation, the correct RAM data can be detected from the second, but the first data would be incorrect, as there is no time margin to transfer the RAM data. In case of DDRAM reading operation, the cursor shift instruction plays the same role as DDRAM address set instruction also transfers RAM data to output data register. After read operation address counter is automatically increased / decreased by 1 according to the entry mode. After CGRAM read operation is, the display shift may not be executed correctly.

\* In case of RAM write operation, AC is increased / decreased by 1 like read operation (after this operation) . In this time, AC indicates the next address position, but only the previous data can be read by read instruction.

## 2. INTERFACE with MPU

### 2-1. Interface with 8-bit MPU

With 8-bit interfacing data length transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.

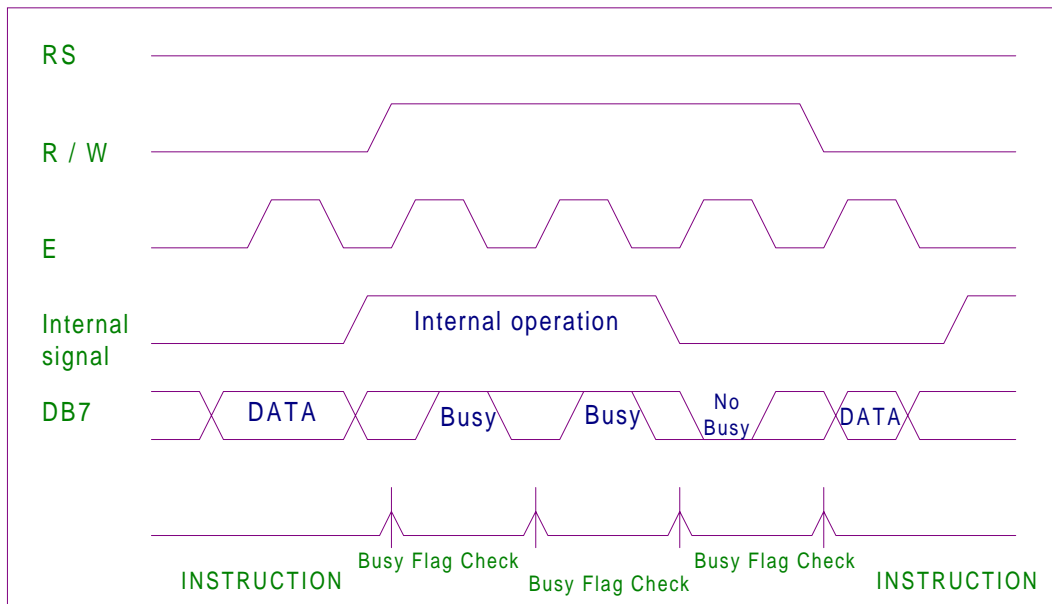


Fig 1. Example of 8-bit Bus Mode Timing Diagram

## 2-2. Interface with 4-bit MPU

When interfacing data lengths are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4-DB7) are transferred, then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0-DB3) are transferred. So transfer is performed twice. Busy Flag outputs “High” after the second transfer are ended. Example of timing sequence is shown below.

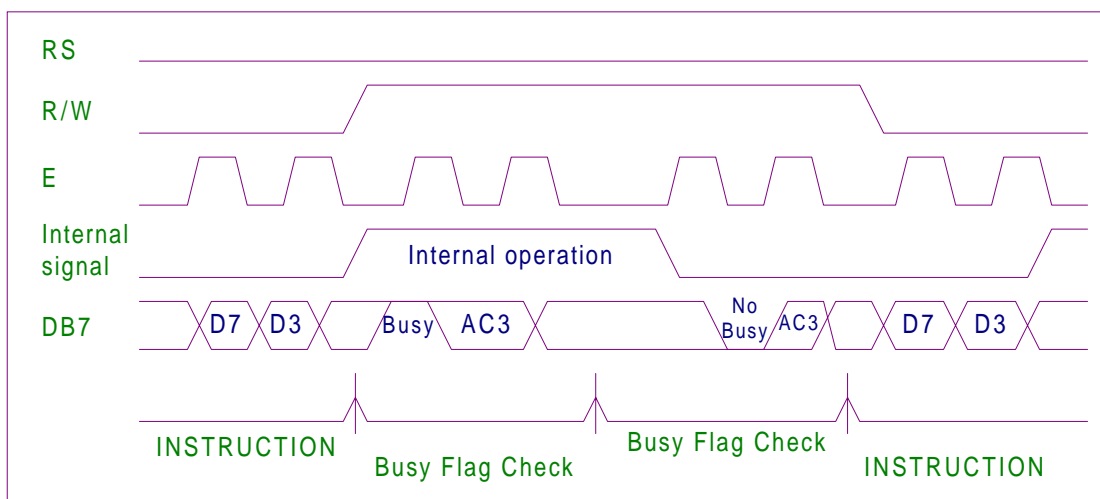


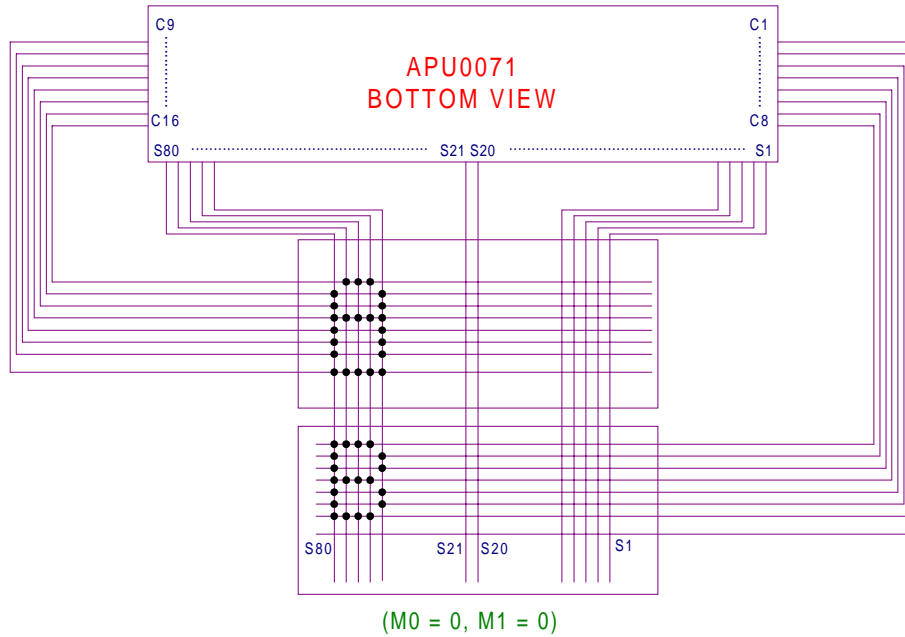
Fig 2. Example of 4-bit Bus Mode Timing Diagram



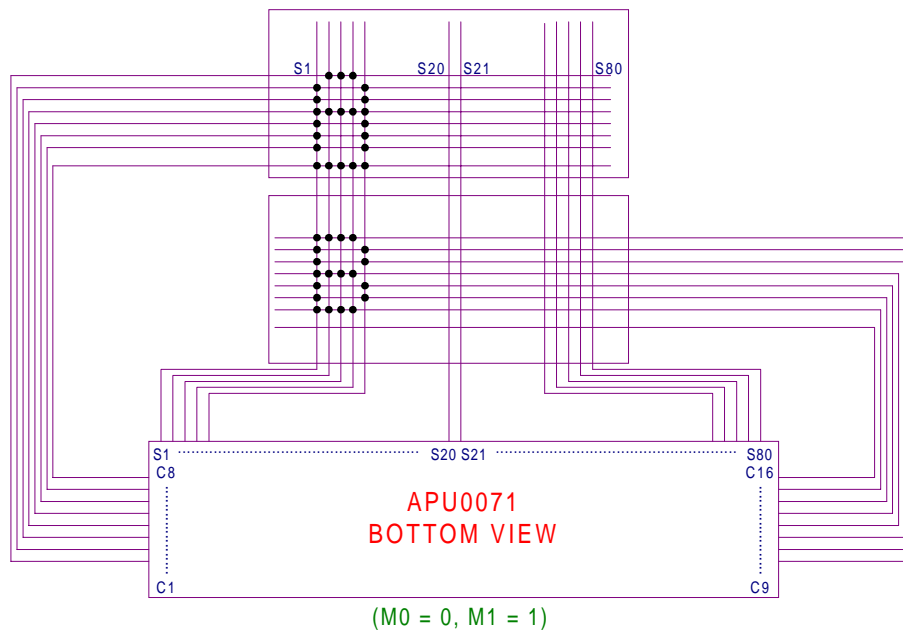
**APPLICATION INFORMATION**

**1. COM / SEG output rotation mode A**

**1-1. DDRAM address mode 1 (A = 1) (2 Line)**

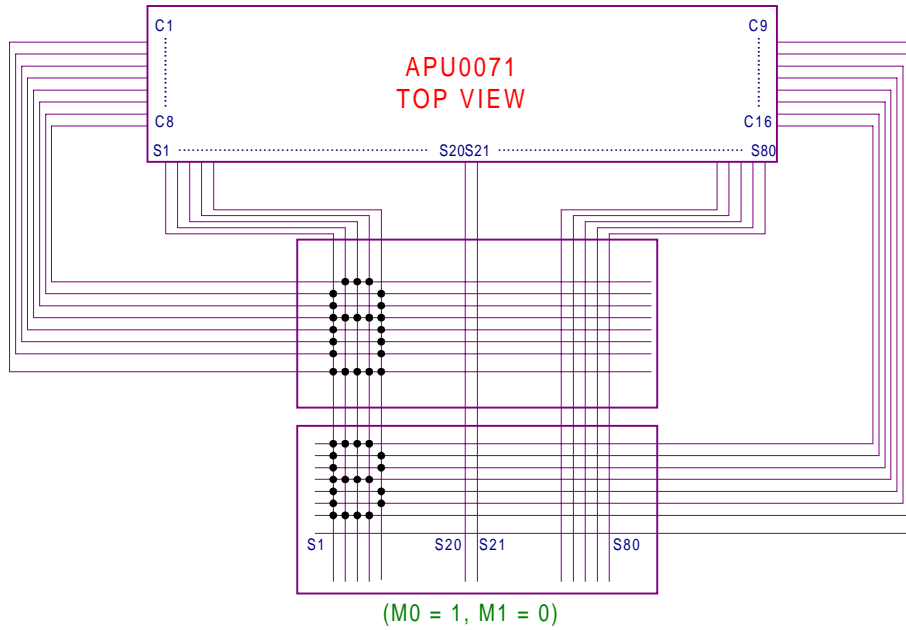


**1-2. DDRAM address mode 1 (A = 1) (2 Line)**

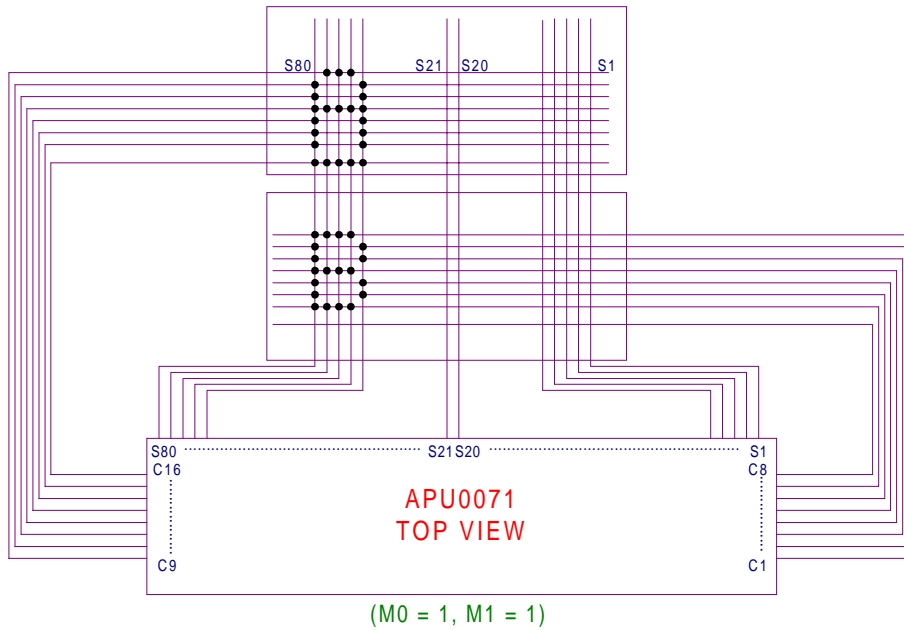


**2. COM / SEG output rotation mode B**

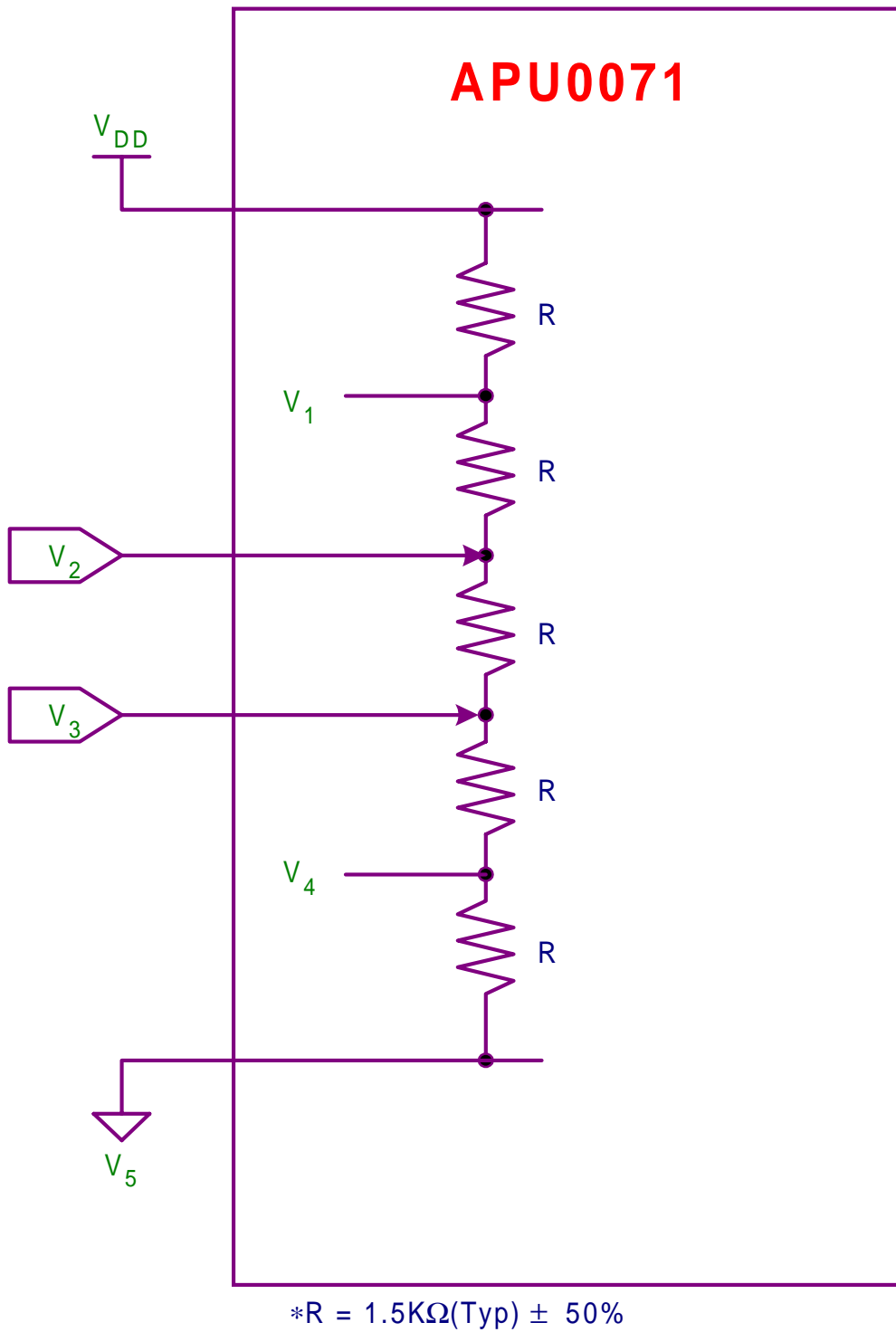
**2-1. DDRAM address mode 1 (A = 1) (2 Line)**



**2-2. DDRAM address mode 1 (A = 1) (2 Line)**



3. POWER SUPPLY for DRIVING LCD PANEL



## INITIALIZING

### 1. INITIALIZE BY INTERNAL POWER-ON-RESET CIRCUIT

When the power is turned on, APU0071 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) up to the end of initialization.

### 2. POWER ON INITIALIZE FLOW

#### 2-1 . Display Clear

Write "20H" to all DDRAM

#### 2-2 . Set Functions

DL = 1 : 8-bit bus mode

A = 1 : 2 Line

M0 = 0 : No Rotation

M1 = 1 : Bottom view mode

#### 2-3 . Control Display ON / OFF instruction

D = 0 : Display OFF

C = 0 : Cursor OFF

B = 0 : Blink OFF

#### 2-4 . Set Entry Mode

I / D = 1 : Increment by 1

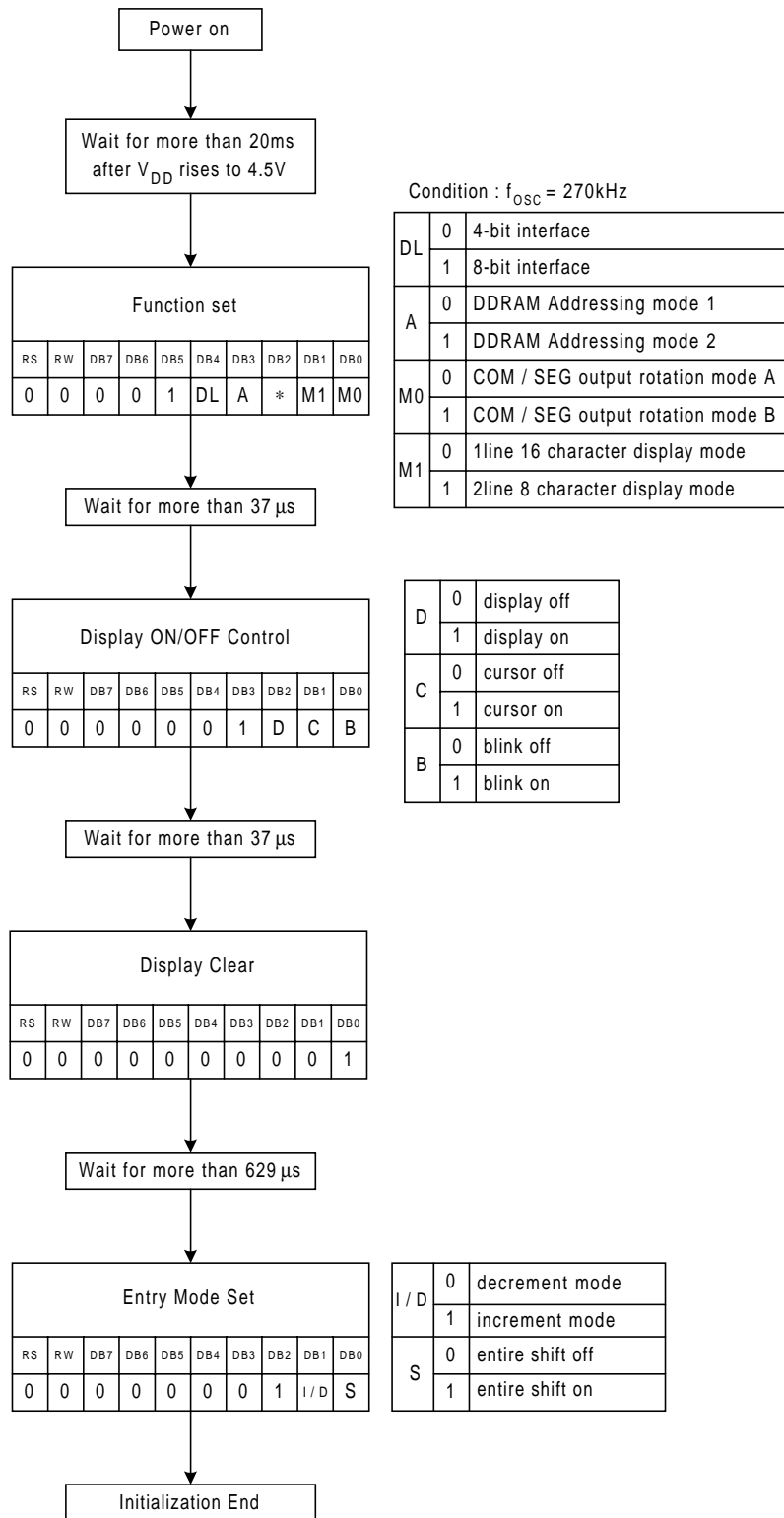
S = 0 : No entire display shift

### 3. INITIALIZE BY EXTERNAL HARDWARE RESET

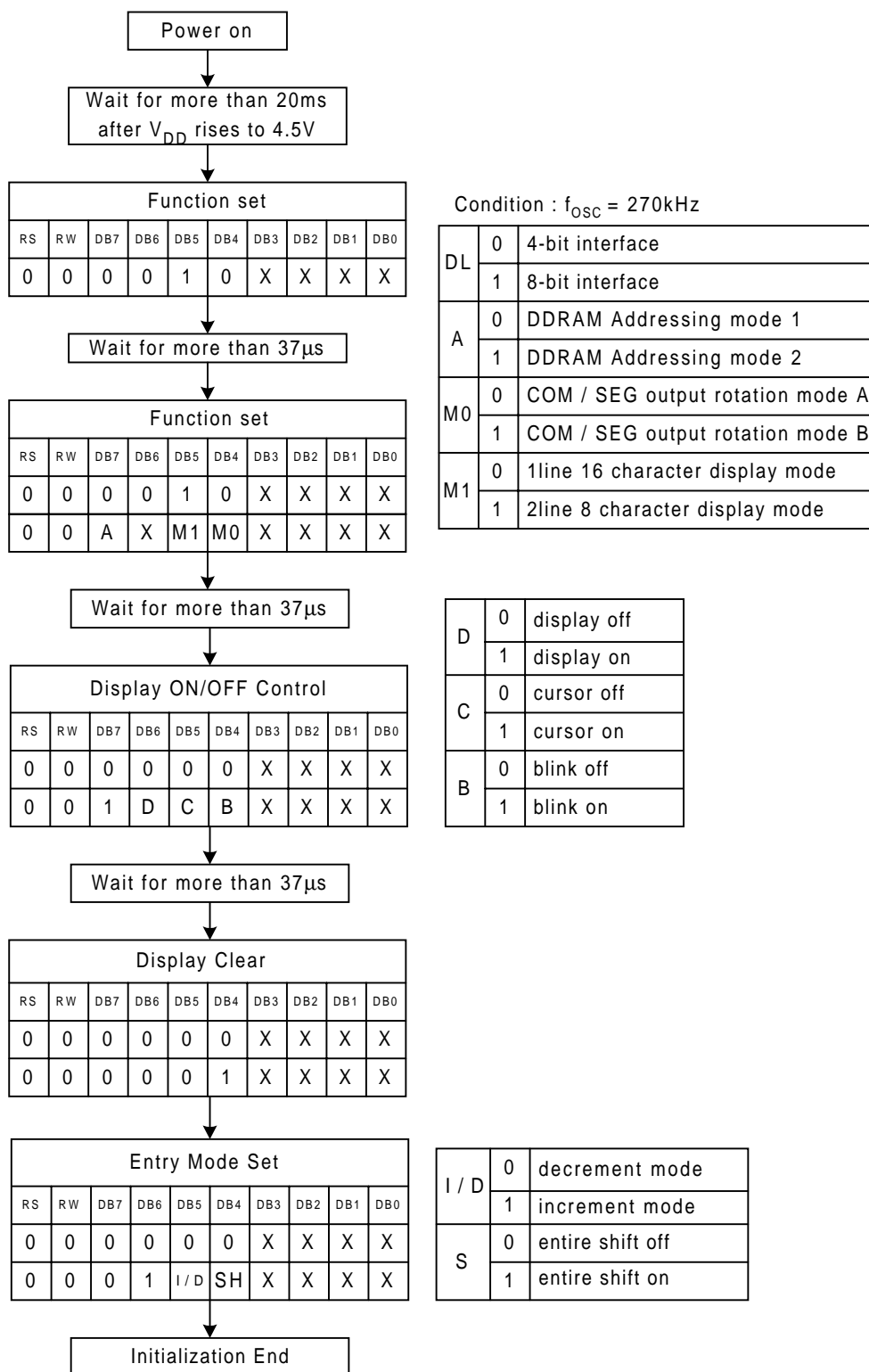
If the "Low" signal is forced to reset terminal over a period of 1.2 ms then system will be initialized. And BF (Busy Flag) is kept "High" (busy state) for 629 us after releasing the initializing sequence.

## 4. INITIALIZING BY INSTRUCTION

### 4-1. 8-bit interface mode

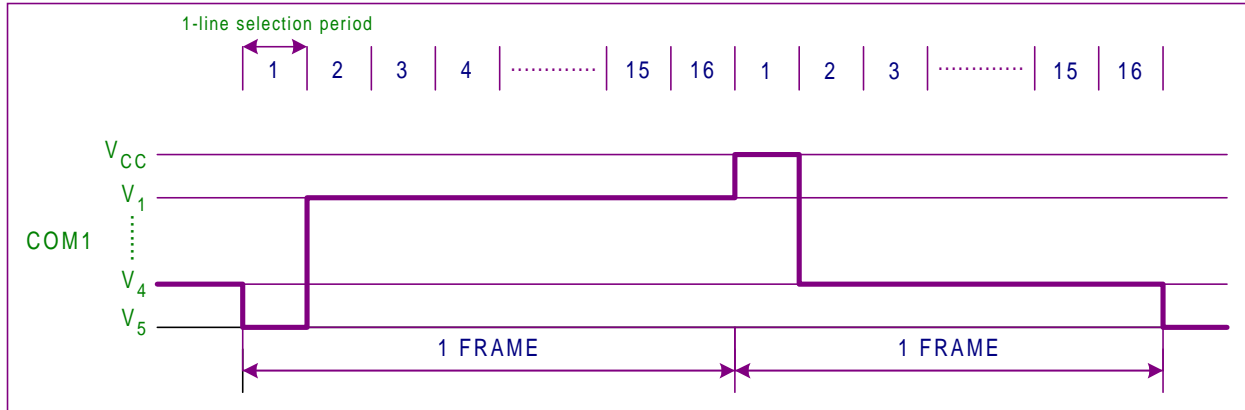


## 4-2. 4-bit interface mode



## Frame frequency

1/16 duty cycle



1-Line selection period = 160 clocks

One Frame =  $40 \times 16 \times 3.7\mu\text{s} \times 4 = 9.472\text{ms}$  (1 CLOCK =  $3.7\mu\text{s}$  at  $f_{\text{osc}} = 270\text{KHz}$ )

Frame frequency =  $1 / 9.472\text{ms} = 105.6\text{Hz}$

## Maximum absolute limit

Maximum absolute Power Ratings

\*Voltage greater than above may damage to the circuit ( $V_{DD} \geq V_2 \geq V_3 \geq V_5$ ,  $V_{LCD} = V_{DD} - V_5$ )

Item	Symbol	Unit	Value
Power supply voltage (1)	$V_{DD}$	V	-0.3 to +7.0
Power supply voltage (2)	$V_{LCD}$	V	-0.3 to +7.0
Input voltage	$V_{IN}$	V	-0.3 to $V_{DD} + 0.3$

## Temperature Characteristics

Item	Symbol	Unit	Value
Operation temperature	$T_{opr}$	°C	-30 to +85
Storage temperature	$T_{stg}$	°C	-55 to +125

## Electrical characteristics

### DC Characteristics

( $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_a = -30$  to  $+85^{\circ}C$ )

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	—	4.5	—	5.5	V
Supply Current	$I_{DD}$	Internal oscillation ( $V_{DD} = 5.0V$ , $f_{OSC} = 270KHz$ )	—	1.0	1.8	mA
Input Voltage (1) (EXTCLK)	$V_{IH1}$	—	$0.7V_{DD}$	—	$V_{DD}$	V
	$V_{IL1}$	—	-0.3	—	0.8	
Input Voltage (2) (EXTCLK)	$V_{IH2}$	—	$V_{DD} - 1.0$	—	$V_{DD}$	V
	$V_{IL2}$	—	-0.2	—	1.0	
Input Voltage (2) (E pin)	$V_{IH3}$	—	$0.8 V_{DD}$	—	$V_{DD}$	V
	$V_{IL3}$	—	V	—	$0.2 V_{DD}$	
Output Voltage (1) (DB0 to DB7)	$V_{OH1}$	$I_{OH} = -0.205$ (mA)	2.4	—	—	V
	$V_{OL1}$	$I_{OL} = 1.6$ (mA)	V	—	0.4	
Output Voltage (2) (except DB0 to DB7)	$V_{OH2}$	$I_O = -40$ ( $\mu A$ )	$0.9 V_{DD}$	—	V	V
	$V_{OL2}$	$I_O = 40$ ( $\mu A$ )	—	—	$0.1 V_{DD}$	
Voltage Drop	$V_{dCOM}$	$I_O = \pm 0.1$ (mA)	—	—	1	V
	$V_{dSEG}$		—	—	1	
Input Leakage Current	$I_{IL}$	$V_{IN} = 0V$ to $V_{DD}$	-1	—	1	$\mu A$
Low Input Current	$I_{IN}$	$V_{IN} = 0V$ , $V_{DD} = 5V$ (PULL UP)	-50	-125	-250	$\mu A$
LCD Driving Voltage	$V_2$	$V_{DD} = 5V$ , $V_5 = 0V$ SEG output port	2.7	3.0	3.3	V
	$V_3$		1.7	2.0	2.3	
Divide Resistor	$R_B$	$V_{DD} - V_5 = 5V$ $R_B = (V_{DD} - V_5) / I_B$ $I_B =$ Divide Resistor Current	3.7	7.5	11.5	K $\Omega$
Internal Clock (internal Rf)	$f_{IC}$	$V_{DD} = 5V$	190	270	350	KHz
LCD Driving Voltage	$V_{LCD}$	$V_{DD} - 5V$	3.0	—	7.0	V



$(V_{DD} = 2.7V \text{ to } 4.5V, T_a = -30 \text{ to } +85^\circ C)$ 

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	—	2.7	—	4.5	V
Supply Current	$I_{DD}$	Internal oscillation ( $V_{DD} = 3.0V, f_{OSC} = 270KHz$ )	—	0.5	1.2	mA
Input Voltage (1) (except OSC1)	$V_{IH1}$	—	$0.7V_{DD}$	—	$V_{DD}$	V
	$V_{IL1}$	—	-0.3	—	0.4	
Input Voltage (2) (OSC1)	$V_{IH2}$	—	$V_{DD} - 1.0$	—	$V_{DD}$	V
	$V_{IL2}$	—	-0.2	—	$0.2 V_{DD}$	
Input Voltage (2) (E pin)	$V_{IH3}$	—	$0.8 V_{DD}$	—	$V_{DD}$	V
	$V_{IL3}$	—	—	—	0.4	
Output Voltage (1) (DB0 to DB7)	$V_{OH1}$	$I_{OH} = -0.1 \text{ (mA)}$	$0.75 V_{DD}$	—	—	V
	$V_{OL1}$	$I_{OL} = 1.1 \text{ (mA)}$	—	—	$0.2 V_{DD}$	
Output Voltage (2) (except DB0 to DB7)	$V_{OH2}$	$I_O = -40 \text{ (}\mu A)$	$0.8 V_{DD}$	—	—	V
	$V_{OL2}$	$I_O = 40 \text{ (}\mu A)$	—	—	$0.2 V_{DD}$	
Voltage Drop	$V_{dCOM}$	$I_O = \pm 0.1 \text{ (mA)}$	—	—	1	V
	$V_{dSEG}$	$V_{LCD} = 5V$	—	—	1	
Input Leakage Current	$I_{IL}$	$V_{IN} = 0V \text{ to } V_{DD}$	-1	—	1	$\mu A$
Low Input Current	$I_{IN}$	$V_{IN} = 0V, V_{DD} = 3V$ (PULL UP)	-10	-50	-120	$\mu A$
LCD Driving Voltage	$V_2$	$V_{DD} = 3V, V_5 = -2V$ SEG output port	0.7	1.0	1.3	V
	$V_3$		-1.7	0	0.3	
Divide Resistor	$R_B$	$V_{DD} - V_5 = 5V$ $R_B = (V_{DD} - V_5) / I_B$ $I_B = \text{Divide Resistor Current}$	3.7	7.5	11.5	K $\Omega$
Internal Clock (internal Rf)	$f_{IC}$	$V_{DD} = 3V$	190	270	350	KHz
LCD Driving Voltage	$V_{LCD}$	$V_{DD} - 5V$	3.0	—	7.0	V

## Customer Service

### Anpec Electronics Corp.

Head Office :

5F, No. 2 Li-Hsin Road, SBIP,

Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

7F, No. 137, Lane 235, Pac Chiao Rd.,

Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.

Tel : 886-2-89191368

Fax : 886-2-89191369

AC Characteristics

( $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_a = -30$  to  $+85^{\circ}C$ )

Mode	Item	Symbol	Min	Typ	Max	Unit
Write Mode (Refer to Fig-3)	E Cycle Time	$t_C$	500	—	—	ns
	E Rise / Fall Time	$t_r, t_f$	—	—	20	
	E Pules Width (High, Low)	$t_W$	230	—	—	
	R / W and RS Setup Time	$t_{SU1}$	40	—	—	
	R / W and RS Hold Time	$t_{h1}$	10	—	—	
	Data Setup Time	$t_{SU2}$	80	—	—	
	Data Hold Time	$t_{h2}$	10	—	—	
Read Mode (Refer to Fig-4)	E Cycle Time	$t_C$	500	—	—	ns
	E Rise / Fall Time	$t_r, t_f$	—	—	20	
	E Pules Width (High, Low)	$t_W$	230	—	—	
	R / W and RS Setup Time	$t_{SU}$	40	—	—	
	R / W and RS Hold Time	$t_h$	10	—	—	
	Data Setup Time	$t_D$	—	—	120	
	Data Hold Time	$t_{DH}$	20	—	—	

( $V_{DD} = 2.7V$  to  $4.5V$ ,  $T_a = -30$  to  $+85^{\circ}C$ )

Mode	Item	Symbol	Min	Typ	Max	Unit
Write Mode (Refer to Fig-3)	E Cycle Time	$t_C$	1000	—	—	ns
	E Rise / Fall Time	$t_r, t_f$	—	—	25	
	E Pules Width (High, Low)	$t_W$	450	—	—	
	R / W and RS Setup Time	$t_{SU1}$	60	—	—	
	R / W and RS Hold Time	$t_{h1}$	20	—	—	
	Data Setup Time	$t_{SU2}$	195	—	—	
	Data Hold Time	$t_{h2}$	10	—	—	
Read Mode (Refer to Fig-4)	E Cycle Time	$t_C$	1000	—	—	ns
	E Rise / Fall Time	$t_r, t_f$	—	—	25	
	E Pules Width (High, Low)	$t_W$	450	—	—	
	R / W and RS Setup Time	$t_{SU}$	60	—	—	
	R / W and RS Hold Time	$t_h$	20	—	—	
	Data Setup Time	$t_D$	—	—	360	
	Data Hold Time	$t_{DH}$	5	—	—	

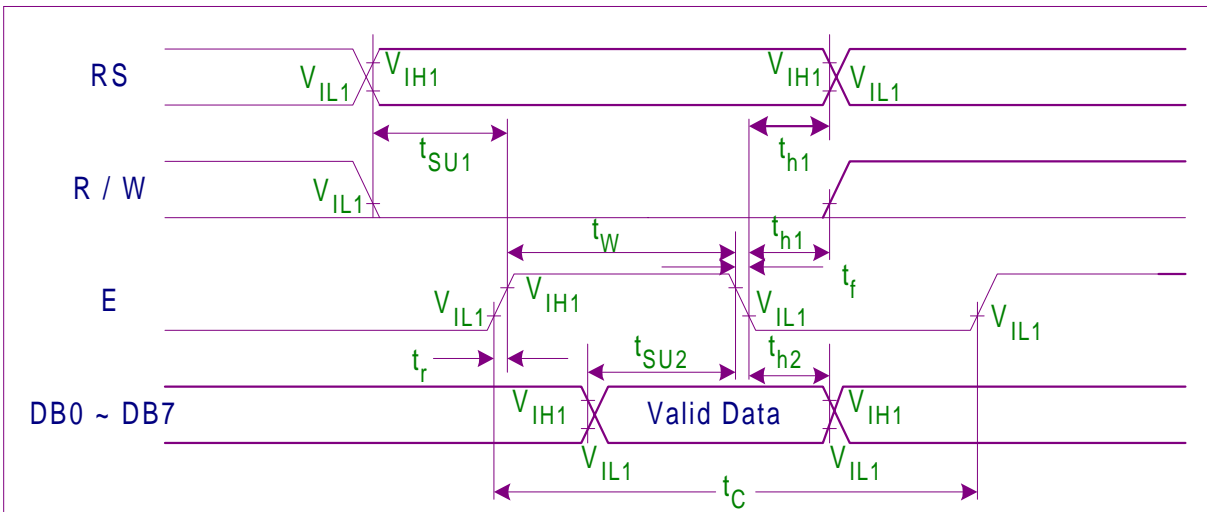


Fig-3. Write Mode Timing Diagram

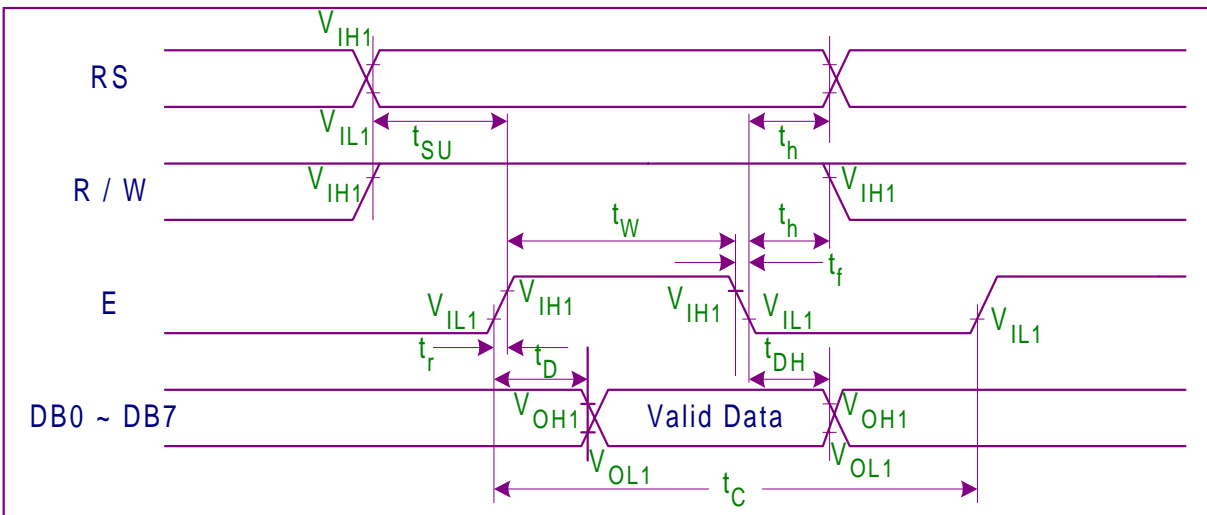


Fig-4. Read Mode Timing Diagram

	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CG RAM (1)															
XXXX0001	CG RAM (2)															
XXXX0010	CG RAM (3)															
XXXX0011	CG RAM (4)															
XXXX0100	CG RAM (5)															
XXXX0101	CG RAM (6)															
XXXX0110	CG RAM (7)															
XXXX0111	CG RAM (8)															
XXXX1000	CG RAM (1)															
XXXX1001	CG RAM (2)															
XXXX1010	CG RAM (3)															
XXXX1011	CG RAM (4)															
XXXX1100	CG RAM (5)															
XXXX1101	CG RAM (6)															
XXXX1110	CG RAM (7)															
XXXX1111	CG RAM (8)															