16 COM / 40 SEG Driver & Controller for Dot Matrix LCD

FEATURES

- Internal Memory
  - Character Generator ROM : 8320 bits
  - Character Generator RAM : 512 bit
  - Display Data RAM : 80 × 8 bits for 80 digits
- Power Supply Voltage : 3V/5V ± 10%
- Supply Voltage for Display : 0 ~ -5V (V_5)
- CMOS Process
- 1/8 duty, 1/11 duty or 1/16 duty : Selectable
  - 1/8 duty : 5 × 7dots format 1 line
  - 1/11 duty: 5 × 10 dots format 1 line
  - 1/16 duty : 5 × 7dots format 2 line
- 80 QFP or Bare Chip Available
- Display Character Pattern :
  - 5 × 7dots format : 192 kinds
  - 5 × 10 dots format : 32 kinds

  (The special character pattern can be programmable by Character Generator RAM directly.)
- A Customer Character Pattern Can be Programmable by Mask Option
- Automatic Power on Reset Function
- It is Possible to Read Both Character Generator and Display Data RAM from MPU

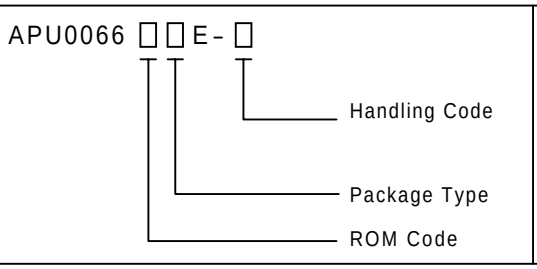
APPLICATIONS

- Character Type Dot Matrix LCD Driver & Con -troller
- Internal Driver :16 Common and 40 Segment Signal Output
- Display Character Format : 5× 7 dots + Cursor, 5 × 10 dots + Cursor
- Easy Interface with a 4-bit or 8-bit MPU

GENERAL DESCRIPTION

The APU0066 is a dot matrix LCD driver & controller LSI that is fabricated by low power CMOS technology.

ORDERING INFORMATION

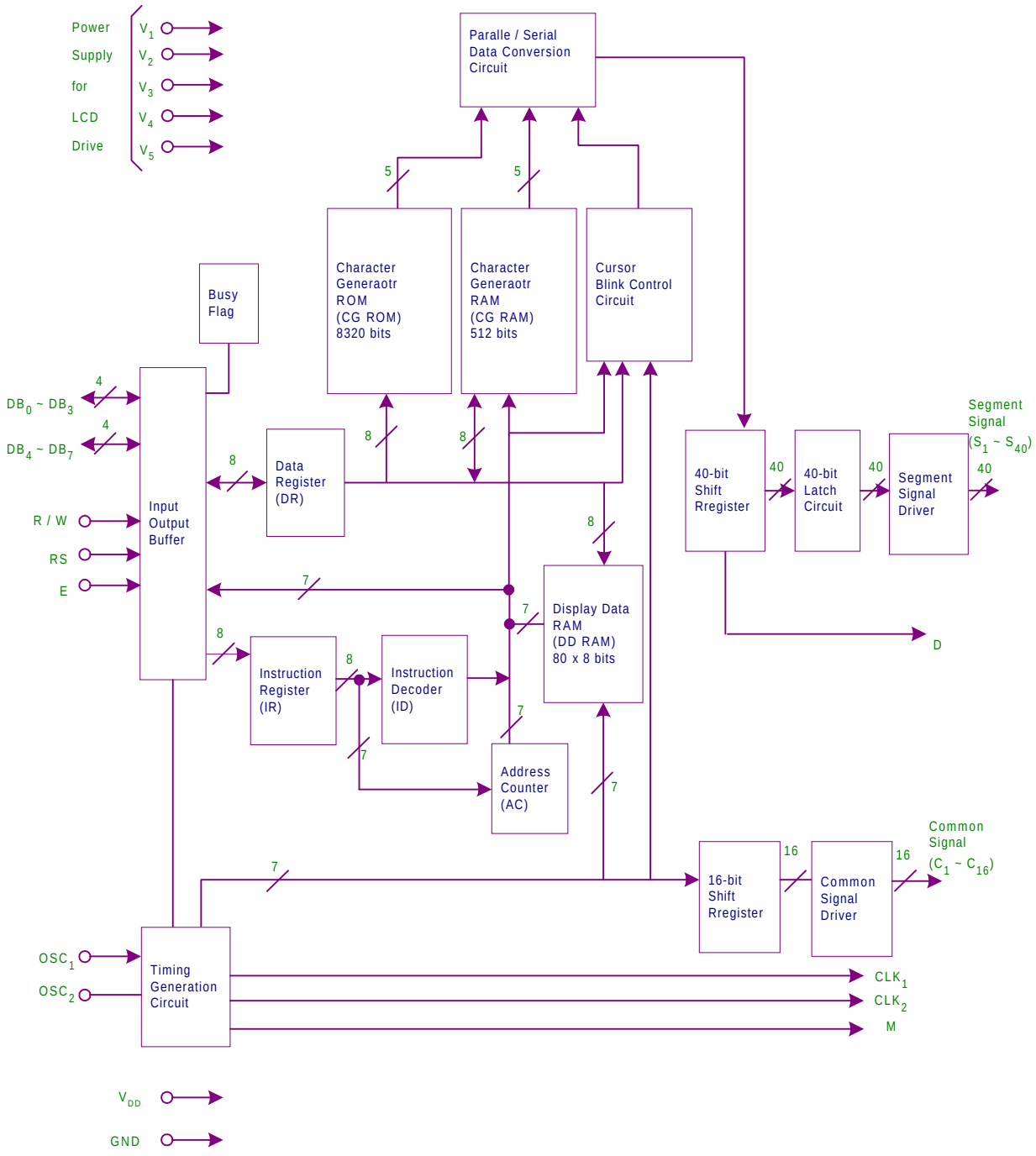


ROM Code
001 : Standard
002 : Customer

Package Type
Q : QFP
Y : Chip

Handling Code
TY : Tray

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS T_A = 25°C

Symbol	Parameter	Rating	Unit
V_{DD}	Operating Voltage	-0.3 ~ +7	V
V_{LCD}	Driver Supply Voltage	V_{DD} - 13.5 ~ V_{DD} + 0.3	V
V_{IN}	Input Voltage	-0.3 ~ V_{DD} + 0.3	V
P_D	Power Dissipation	500	mW
T_{OPR}	Operating Temperature	-20 to +75	°C
T_{STG}	Storage Temperature Range	-30 to +85	°C

∗ Voltage greater than above may damage to the circuit ($V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$)

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD} = 3V ± 10%, V_{SS} = 0V, T_A = -30 ~ 85°C)

Symbol	Parameter	Test Conditions		APU0066 Min.	APU0066 Typ.	APU0066 Max.	Unit	Applicable Pin
V_{DD}	Operating Voltage	—		2.7	3	3.3	V	
I_{DD1}	Operating Current (∗1)	Ceramic Resonator F_{OSC} = 250KHz		—	0.3	0.5	mA	
I_{DD2}		Resistor Oscillation External Clock Operation F_{OSC} = 270KHz		—	0.17	0.3		
V_{IH1}	Input Voltage 1	—	High	1.9	—	V_{DD}	V	E, DB_0 - DB_7 R/W, RS
V_{IL1}			Low	-0.3	—	0.4		
V_{IH2}	Input Voltage 2	—	High	0.7V_{DD}	—	V_{DD}		OSC_1
V_{IL2}			Low	—	—	0.2V_{DD}		
V_{OH1}	Output Voltage 1	I_{OH} = -0.1 mA	High	2.0	—	—		DB_0 - DB_7
V_{LH1}		I_{OL} = 0.1mA	Low	—	—	0.4		
V_{OH2}	Output Voltage 2	I_O = -40µA	High	0.8V_{DD}	—	—		CLK1, CLK2. M, D
V_{LH2}		I_O = 40µA	Low	—	—	0.2V_{DD}		
VD_{COM}	Voltage Drop (∗2)	I_O = ± 0.05mA	COM	—	—	1		C_1 ~ C_{16} S_1 ~ S_{40}
VD_{SEG}			SEG	—	—	1.5		
I_{LKG}	Input Leakage Current	V_{IN} = 0 or V_{DD}		-1	—	1	µA	E
I_{IL}	Input Low Current	V_{DD} = 3V (test pull up R)		-10	-50	-120		RS, R/W, DB_0 - DB_7
F_{EC}	External Clock		Frequency(∗3)	125	250	350	KHz	OSC_1
Duty			Duty	45	50	55	%	
T_R			Rise Time	—	—	0.2	µs	
T_F			Fall Time	—	—	0.2	µs	
F_{OSC}	Internal Clock Frequency (∗3)	Rf = 75K Ω ± 2%		190	270	350	KHz	OSC_1, OSC_2
V_{LCD1}	LCD Driving Voltage (∗4)	V_{DD} – V_5	1/5 bias	3	—	10	V	V_1 – V_5
V_{LCD2}			1/4 bias	3	—	10		

Note: ∗1 : The supply current value from V_{DD} when the power condition is as follows

V_{DD} = 5V, V_{SS} = 0V, V_5 = -2V (when V_{DD} = 5V)

V_{DD} = 3V, V_{SS} = 0V, V_5 = -2V (when V_{DD} = 3V)

∗2 : The voltage drop from LCD bias terminals V_{DD}, V_1, V_4 and V_5 to each common terminal (C_1 ~ C_{16}). And also the voltage drop from LCD bias terminals V_{DD}, V_2, V_3 and V_5 to each segment terminal (S_1 ~ S_{80}).

∗3 and ∗4 : Refer to oscillator circuit and input the voltage listed in the table below to V_1 ~ V_5.

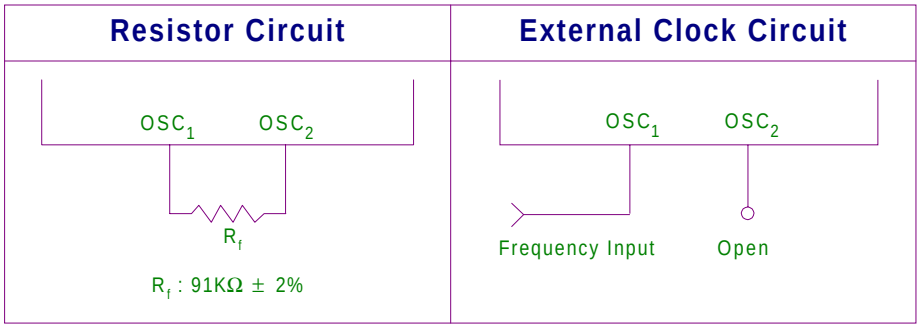
DC Characteristics (V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -20 ~ 75°C)

Symbol	Parameter	Test Conditions		APU0066 Min.	APU0066 Typ.	APU0066 Max.	Unit	Applicable Pin
V_{DD}	Operating Voltage	—		4.5	—	5.5	V	—
I_{DD1}	Operating Current (∗1)	Ceramic Resonator F_{OSC} = 250KHz		—	0.55	0.8	mA	—
I_{DD2}		Resistor Oscillation External Clock Operation F_{OSC} = 270KHz		—	0.35	0.6		
V_{IH1}	Input Voltage 1	—	High	2.2	—	V_{DD}	V	E, DB_0 - DB_7 R/W, RS
V_{IL1}			Low	-0.3	—	0.6		
V_{IH2}	Input Voltage 2	—	High	V_{DD} - 1	—	V_{DD}		OSC_1
V_{IL2}			Low	-0.2	—	1		
V_{OH1}	Output Voltage 1	I_{OH} = -0.205mA	High	2.4	—	—		DB_0 - DB_7
V_{LH1}		I_{OL} = 1.2mA	Low	—	—	0.4		
V_{OH2}	Output Voltage 2	I_O = -40µA	High	0.9V_{DD}	—	—		CLK1, CLK2. M, D
V_{LH2}		I_O = 40µA	Low	—	—	0.1V_{DD}		
VD_{COM}	Voltage Drop (∗2)	I_O = ± 0.1mA	COM	—	—	1		C_1 ~ C_{16}
VD_{SEG}			SEG	—	—	1		S_1 ~ S_{40}
I_{LKG}	Input Leakage Current	V_{IN} = 0 or V_{DD}		-1	—	1	µA	E
I_{IL}	Input Low Current	V_{DD} = 5V (test pull up R)		-50	-125	-250		RS, R/W, DB_0 - DB_7
F_{EC}	External Clock		Frequency (∗3)	125	250	350	KHz	OSC_1
Duty			Duty	45	50	55	%	
T_R			Rise Time	—	—	0.2	µs	
T_F			Fall Time	—	—	0.2	µs	
F_{OSC1}	Internal Clock Frequency (∗3)	Rf = 91K Ω ± 2%		190	270	350	KHz	OSC_1, OSC_2
V_{LCD1}	LCD Driving Voltage (∗4)	V_{DD} - V_5	1/5 bias	4.6	—	10	V	V_1 – V_5
V_{LCD2}			1/4 bias	3	—	10		

Note : ∗1 : Applies to the current value flown in terminal V_{DD} when power is input as follows;
V_{DD} = 5V, GND = 0V, V_1 = 3.4V, V_2 =1.8V, V_3 = 0.2V, V_4 = 1.4V and V_5 = -3V.

∗2 : Applied to the voltage drop occurring from terminals V_{DD} , V_1, V_4 and V_5 to each common terminal (C_1 - C_{16}) when 0.1mA is flown in or out to and from all COM and SEG terminals, and also to voltage drop occurring from terminals V_{DD} ,V_2, V_3 and V_5 to each SEG terminal (S_1 ~ S_{40}). When the output level is at V_{DD} , V_1, V_2 level , 0.1mA is flown out, while 0.1mA flow in when the output level is at V_3, V_4 or V_5 level. This occurs when 5V or -5V is input to V_{DD}, V_1 and V_3 or to V_2, V_4, and V_5 respectively.

∗3 : Oscillator Circuit



∗4 : Input the voltage listed in the table below to V_1 - V_5

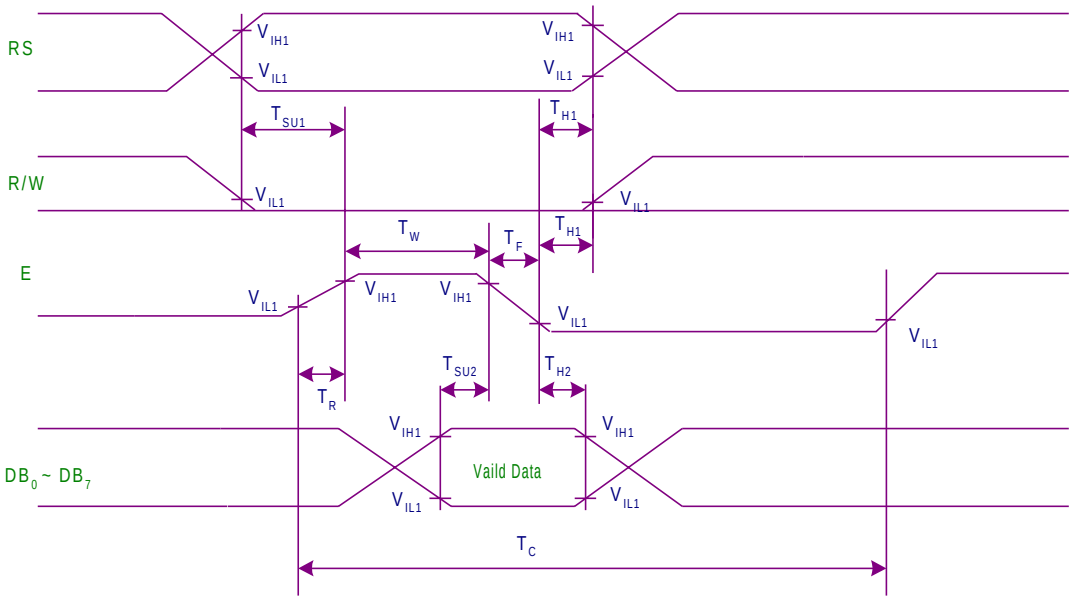
Duty	1/8, 1/11	1/16
Bias	1/4	1/5
Power Supply		
V_1	V_{DD} - V_{LCD} / 4	V_{DD} - V_{LCD} / 5
V_2	V_{DD} - V_{LCD} / 2	V_{DD} - 2V_{LCD} / 5
V_3	V_{DD} - V_{LCD} / 2	V_{DD} - 3V_{LCD} / 5
V_4	V_{DD} - 3V_{LCD} / 4	V_{DD} - 4V_{LCD} / 5
V_5	V_{DD} - V_{LCD}	V_{DD} - V_{LCD}

∗ V_{LCD} is the LCD driving voltage, refer to the initial set of the instruction code.

AC Characteristics (V_{DD} = 5V ± 10%, V_{SS}= 0V, T_A = -20 ~ +75°C)

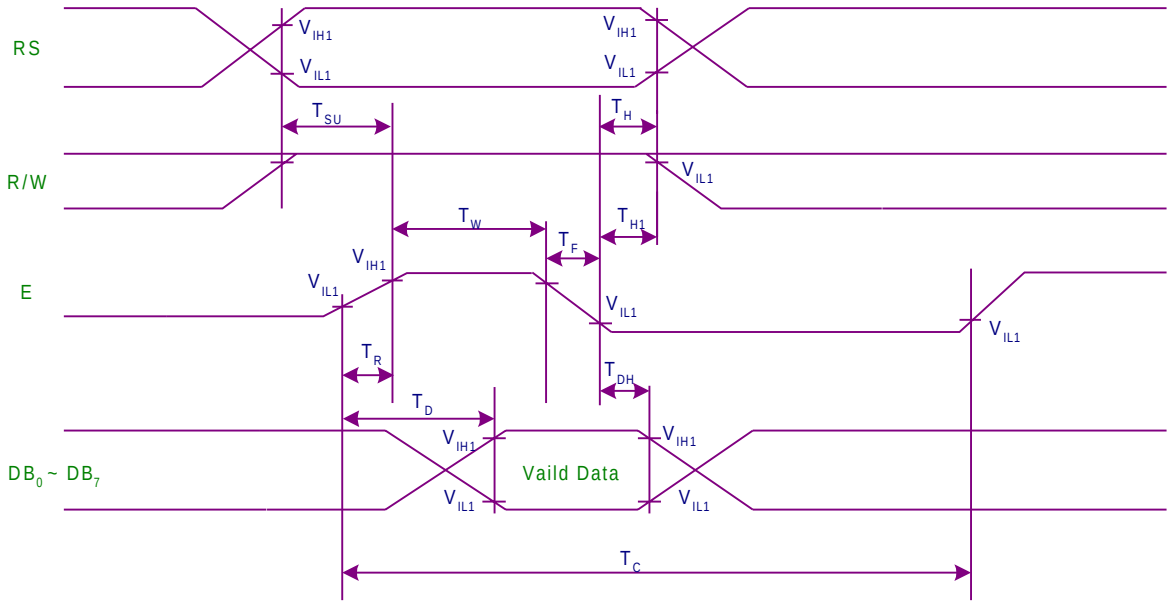
1. Write mode

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Test Pin
T_C	E Cycle Time	500	-	-	ns	E
T_R	E Rise Time	-	-	25	ns	E
T_F	E Fall Time	-	-	25	ns	E
T_W	E Pulse Width (High, Low)	220	-	-	ns	E
T_{SU1}	R/W and RS Set-up Time	40	-	-	ns	R/W, RS
T_{H1}	R/W and RS Hold Time	10	-	-	ns	R/W,RS
T_{SU2}	Data Set-up Time	60	-	-	ns	DB_0 ~ DB_7
T_{H2}	Data Hold Time	10	-	-	ns	DB_0 ~ DB_7



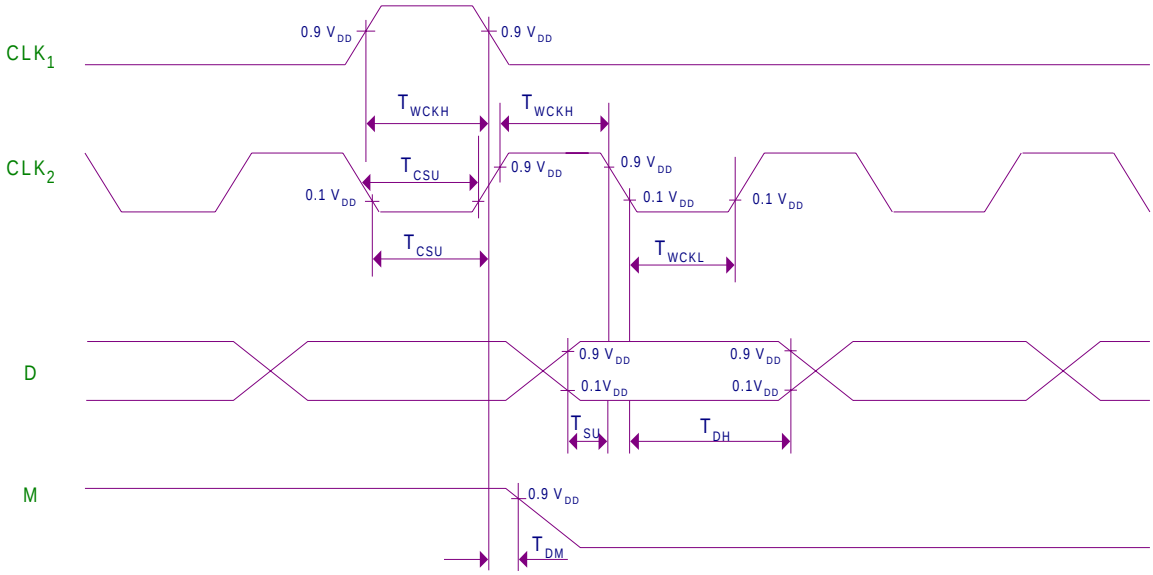
2. Read mode

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Test Pin
T_C	E Cycle Time	500	-	-	ns	E
T_R	E Rise Time	-	-	25	ns	E
T_F	E Fall Time	-	-	25	ns	E
T_W	E Pulse Width (High, Low)	220	-	-	ns	E
T_{SU}	R/W and RS Set-up Time	40	-	-	ns	R/W, RS
T_H	R/W and RS Hold Time	10	-	-	ns	R/W,RS
T_D	Data Output Delay Time	-	-	120	ns	DB_0 ~ DB_7
T_{DH}	Data Hold Time	20	-	-	ns	DB_0 ~ DB_7

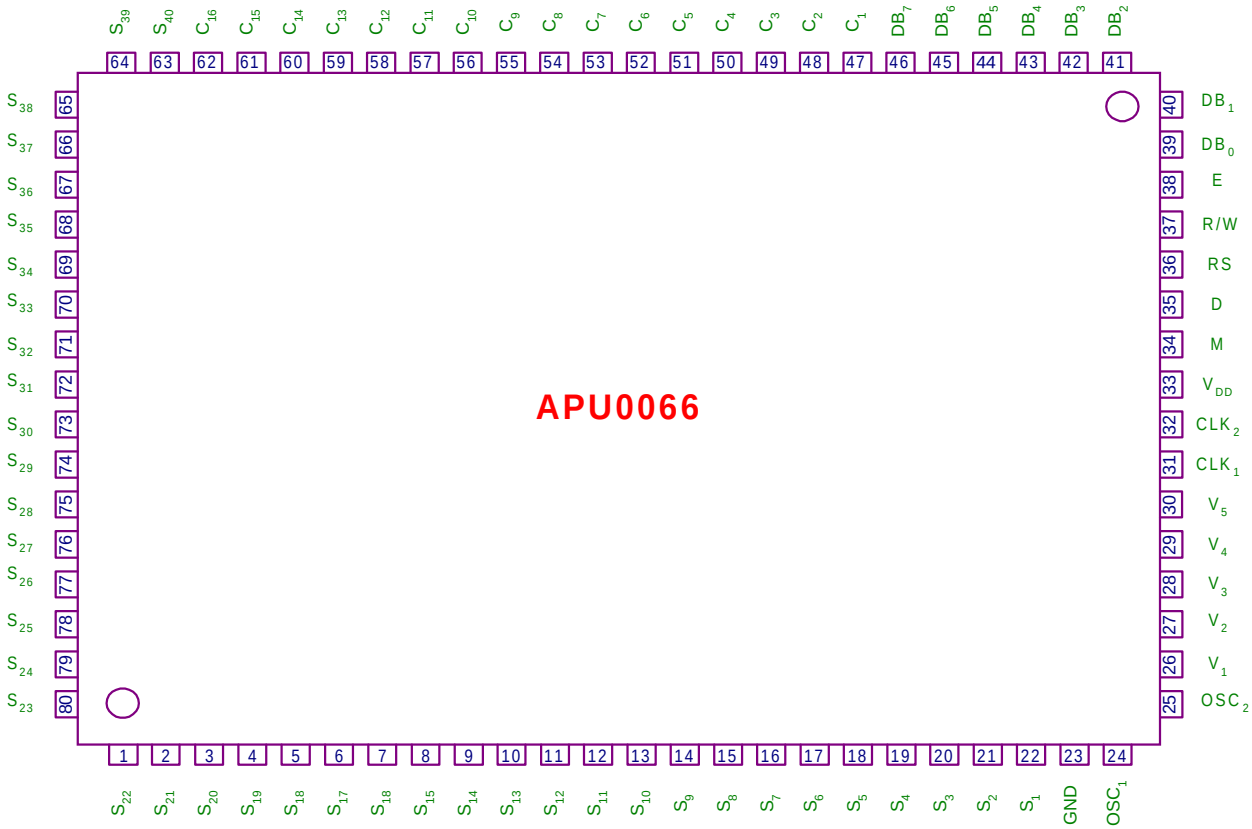


3. Interface mode with APU0065, APU0063

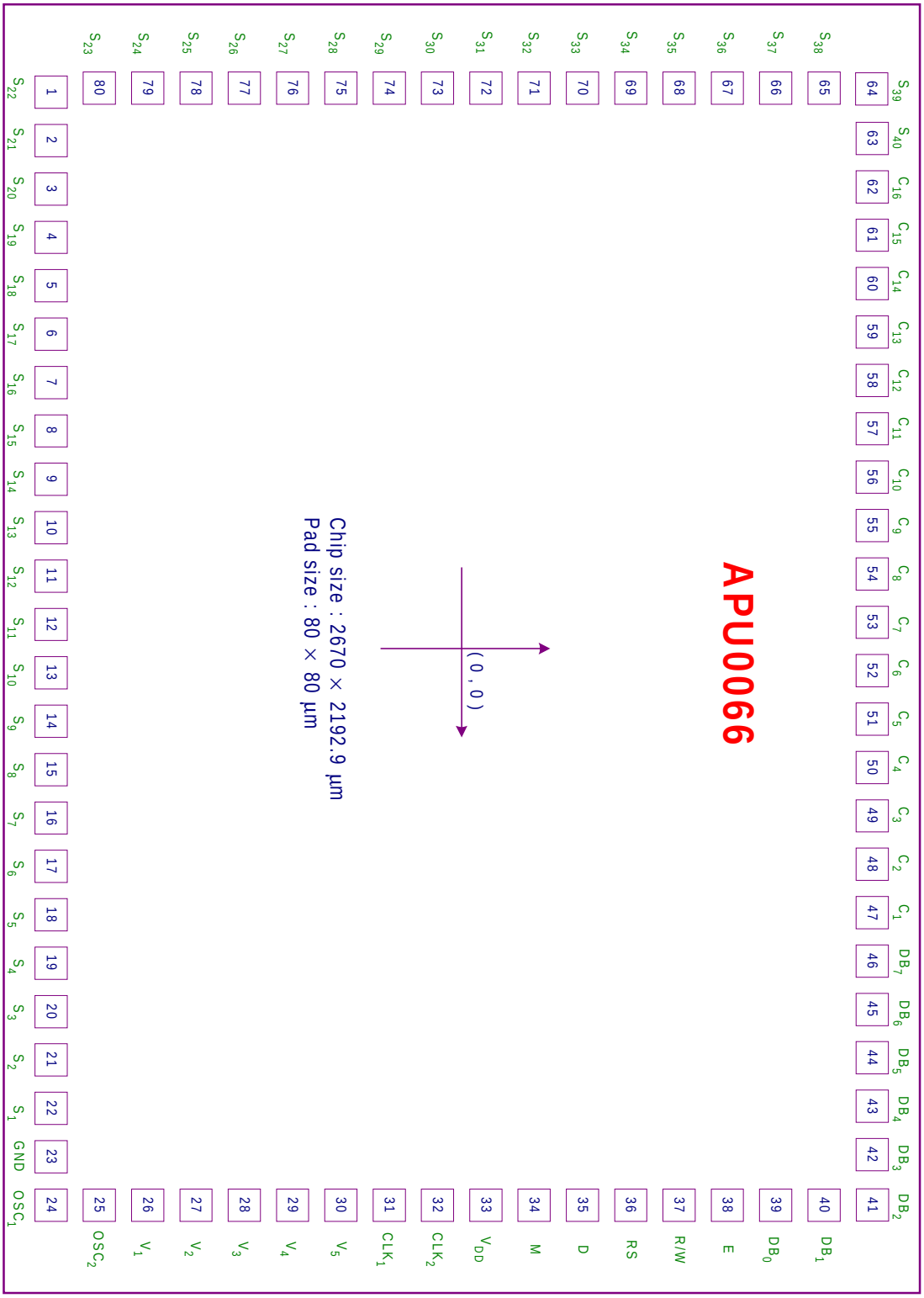
Symbol	Characteristic	Min.	Typ.	Max.	Unit	Test Pin
T_{WCKH}	Clock Pulse Width High	800	-	-	ns	CKL
T_{WCKL}	Clock Pulse Width Low	800	-	-	ns	CLK
T_{SU}	Data Set-up Time	300	-	-	ns	D
T_{DH}	Data Hold Time	300	-	-	ns	D
T_{CSU}	Clock Set-up Time	500	-	-	ns	CLK
T_{DM}	M Delay Time	-1000	-	1000	ns	M



PIN CONFIGURATION _80 QFP TOP VIEW



CHIP PAD ARRANGEMENT



PAD LOCATION

PIN NO.	PIN NAME	X	Y	PIN NO.	PIN NAME	X	Y
1	S_{22}	-1,265.00	-1,025.15	41	DB_2	1,265.00	1,022.65
2	S_{21}	-1,140.00	-1,031.45	42	DB_3	1,140.00	1,031.45
3	S_{20}	-1,015.00	-1,031.45	43	DB_4	1,015.00	1,031.45
4	S_{19}	-890.00	-1,031.45	44	DB_5	890.00	1,031.45
5	S_{18}	-770.00	-1,031.45	45	DB_6	770.00	1,031.45
6	S_{17}	-650.00	-1,031.45	46	DB_7	650.00	1,031.45
7	S_{16}	-550.00	-1,031.45	47	C_1	550.00	1,031.45
8	S_{15}	-450.00	-1,031.45	48	C_2	450.00	1,031.45
9	S_{14}	-350.00	-1,031.45	49	C_3	350.00	1,031.45
10	S_{13}	-250.00	-1,031.45	50	C_4	250.00	1,031.45
11	S_{12}	-150.00	-1,031.45	51	C_5	150.00	1,031.45
12	S_{11}	-50.00	-1,031.45	52	C_6	50.00	1,031.45
13	S_{10}	50.00	-1,031.45	53	C_7	-50.00	1,031.45
14	S_9	150.00	-1,031.45	54	C_8	-150.00	1,031.45
15	S_8	250.00	-1,031.45	55	C_9	-250.00	1,031.45
16	S_7	350.00	-1,031.45	56	C_{10}	-350.00	1,031.45
17	S_6	450.00	-1,031.45	57	C_{11}	-450.00	1,031.45
18	S_5	550.00	-1,031.45	58	C_{12}	-550.00	1,031.45
19	S_4	650.00	-1,031.45	59	C_{13}	-650.00	1,031.45
20	S_3	770.00	-1,031.45	60	C_{14}	-770.00	1,031.45
21	S_2	890.00	-1,031.45	61	C_{15}	-890.00	1,031.45
22	S_1	1,015.00	-1,031.45	62	C_{16}	-1,015.00	1,031.45
23	GND	1,140.00	-1,031.45	63	S_{40}	-1,140.00	1,031.45
24	OSC_1	1,265.00	-1,024.55	64	S_{39}	-1,265.00	1,021.20
25	OSC_2	1,270.00	-811.95	65	S_{38}	-1,270.00	808.05
26	V_1	1,270.00	-691.95	66	S_{37}	-1,270.00	688.05
27	V_2	1,270.00	-571.95	67	S_{36}	-1,270.00	568.05
28	V_3	1,270.00	-451.95	68	S_{35}	-1,270.00	448.05
29	V_4	1,270.00	-351.95	69	S_{34}	-1,270.00	348.05
30	V_5	1,270.00	-251.95	70	S_{33}	-1,270.00	248.05
31	CLK_1	1,270.00	-151.95	71	S_{32}	-1,270.00	148.05
32	CLK_2	1,270.00	-51.95	72	S_{31}	-1,270.00	48.05
33	V_{DD}	1,270.00	48.05	73	S_{30}	-1,270.00	-51.95
34	M	1,270.00	148.05	74	S_{29}	-1,270.00	-151.95
35	D	1,270.00	248.05	75	S_{28}	-1,270.00	-251.95
36	RS	1,270.00	348.05	76	S_{27}	-1,270.00	-351.95
37	R/W	1,270.00	448.05	77	S_{26}	-1,270.00	-451.95
38	E	1,270.00	568.05	78	S_{25}	-1,270.00	-571.95
39	DB_0	1,270.00	688.05	79	S_{24}	-1,270.00	-691.95
40	DB_1	1,270.00	808.05	80	S_{23}	-1,270.00	-811.95

PIN DESCRIPTION-QFP80

Pin (No)	Input / Output	Name	Description	Interface
V_{DD} (33)	Power	Operating Voltage	For logical circuit (+5V ± 10%)	Power Supply
V_{SS} (GND) (23)			0V (GND)	
V_1 - V_5 (26 - 30)		Vegetative Supply Voltage	Bias voltage level for LCD driving	
S_1 - S_{40} (22 - 1, 80 - 63)	Output	Segment Output	Segment signal output for LCD driving	LCD
C_1 - C_{16} (47 - 62)	Output	Common Output	Common signal output for LCD driving	LCD
OSC_1, OSC_2 (24) (25)	Input (OSC_1) Output (OSC_2)	Oscillator	Both pins connected to Rf resistor or ceramic resonator for internal oscillator circuit. In case of external frequency use only, the frequency is input to (OSC_1) terminal.	Resistor or Ceramic Resonator
CLK_1 (31)	Output	Data latch clock	Clock output terminal for the serially transferred data to be latched to the driver.	APU0065 or APU0063
CLK_2 (32)		Data shift clock	Clock output terminal used when D terminal data output shifts the inside of the driver.	
M (34)		Alternated signal for LCD driver output	The alternating signal to convert LCD drive waveform to AC	
D (35)		Display data interface	Character pattern data, which is corresponding, to each common signal, is supplied to driver serially. High: Selection Low: Non selection	
E (38)	Input	Enable	Start enable signal to read or write the data	
R / W (37)		Read / Write	R/W signal input is used to select the read/write mode High: Read mode Low: Write mode	MPU
RS (36)		Register select	Register selection input High: Data register (for read and write) Low: Instruction register (for write), Busy flag, address counter (for read)	
DB_0 - DB_7 (39 - 46)	Input / Output	Data interface	Used for data transfer between the MPU and APU0066. These terminals are for data bus with bi-directional three-state. Initial 4 bit (DB_0 - DB_3) are not used during 4 bit operation (DB_7 can be used as a busy flag)	

Customer Service

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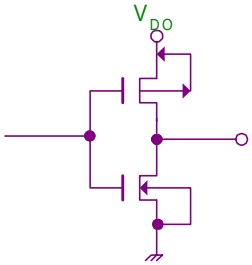
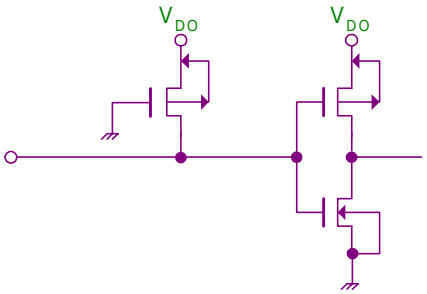
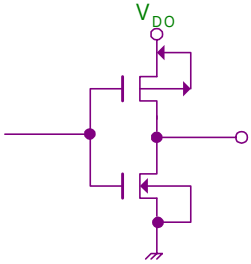
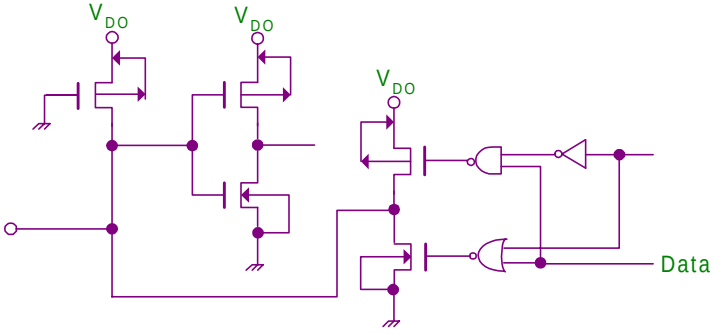
Fax : 886-2-89191369

INTERNAL LOGIC of INPUT / OUTPUT TERMINAL

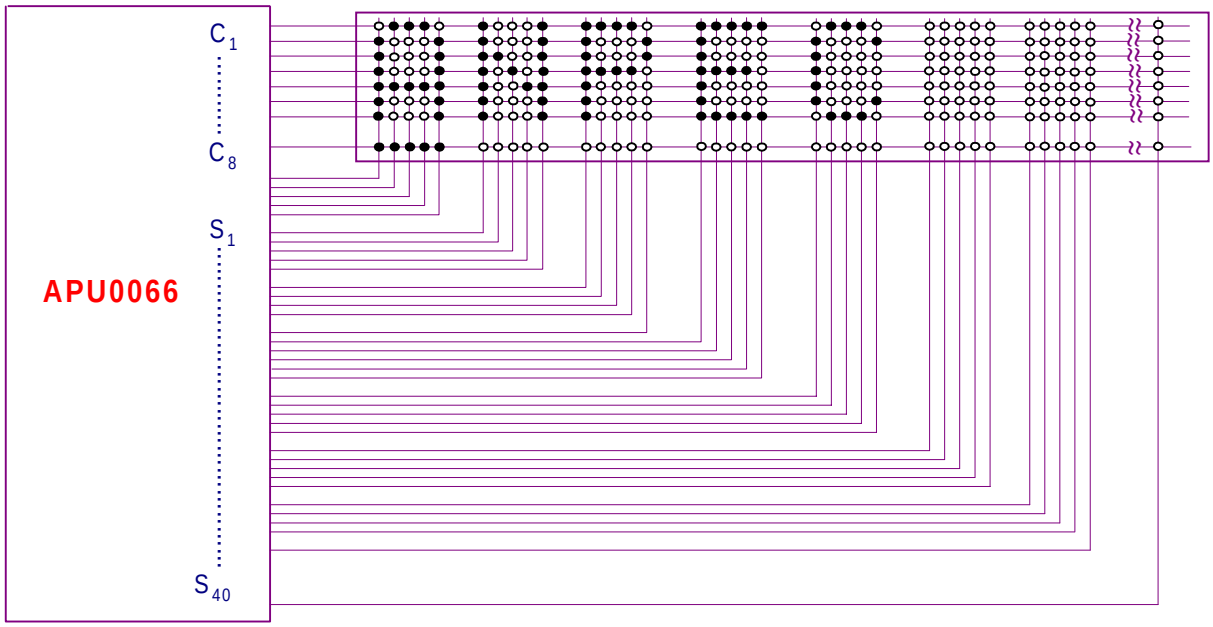
Input / Output		Logic Diagram	Applicable Pin
Input	No Pull Up		E
	With Pull Up		RS, R / W
Input			CLK_1, CLK_2, M, D
Input / Output			DB_0 ~ DB_7

CONTROL and DISPLAY COMMAND

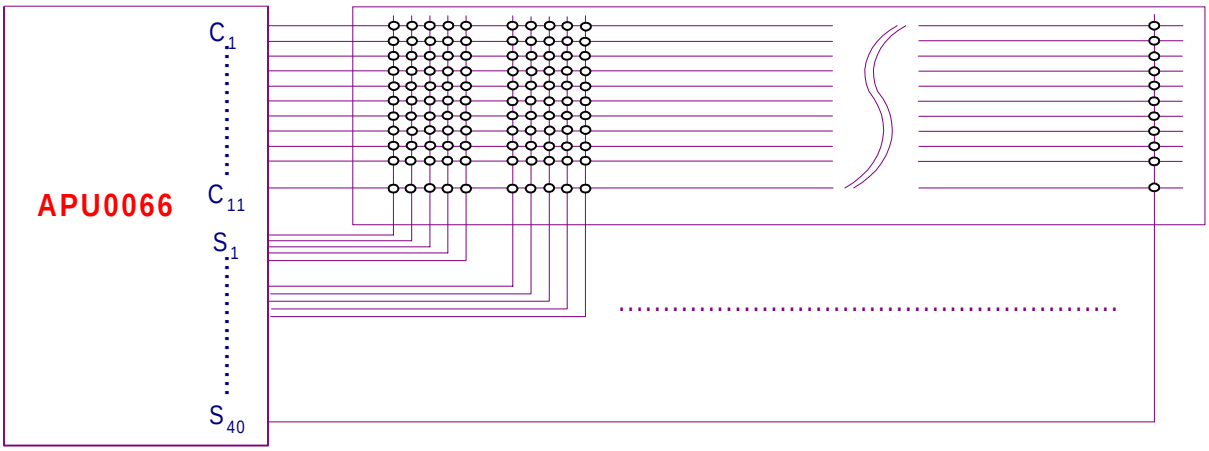
Command	RS	R / W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Execution Time (fosc=250KHz)	Remark
Display Clear	L	L	L	L	L	L	L	L	L	H	1.64ms	
Return Home	L	L	L	L	L	L	L	L	H	X	1.64ms	Cursor move to first digit
Entry Mode Set	L	L	L	L	L	L	L	H	I / D	SH	40µs	I / D : set cursor Move direction H : Increase L : Decrease SH : Specifies shift of display H : display is Shifted L : display is not Shifted
Display ON / OFF	L	L	L	L	L	L	H	D	C	B	40µs	Display H : Display on L : display off Cursor H : Cursor on L : Cursor off Blinking H : Blinking on L : Blinking off
Shift	L	L	L	L	L	H	S / C	R / L	X	X	40µs	SC : H : Display shift L : Cursor move R/L : H : Right shift L : Left shift
Set Function	L	L	L	L	H	DL	N	F	X	X	40µs	DL : H : 8 bits interface L : 4 bits interface N : H : 2 line display L : 1 line display F : H : 5 × 10 dots L : 5 × 7 dots
Set CG RAM Address	L	L	L	H	CG RAM address (corresponds to cursor address)						40µs	CG RAM data is sent and received after this setting
Set DD RAM Address	L	L	H	DD RAM address							40µs	DD RAM data is sent and received after this setting
Write data	H	L	Writ Data								46µs	Write data into DD or CG RAM
Read data	H	H	Read Data								46µs	Read data from DD or CG RAM
Read Busy Flag & Address	L	H	BF	Address counter used for both DD & CG RAM address							0µs	BF : H : Busy L : Ready * Reads BF indication internal operating is being performed. * Reads address counter contents

APPLICATION INFORMATION ACCORDING to LCD PANEL

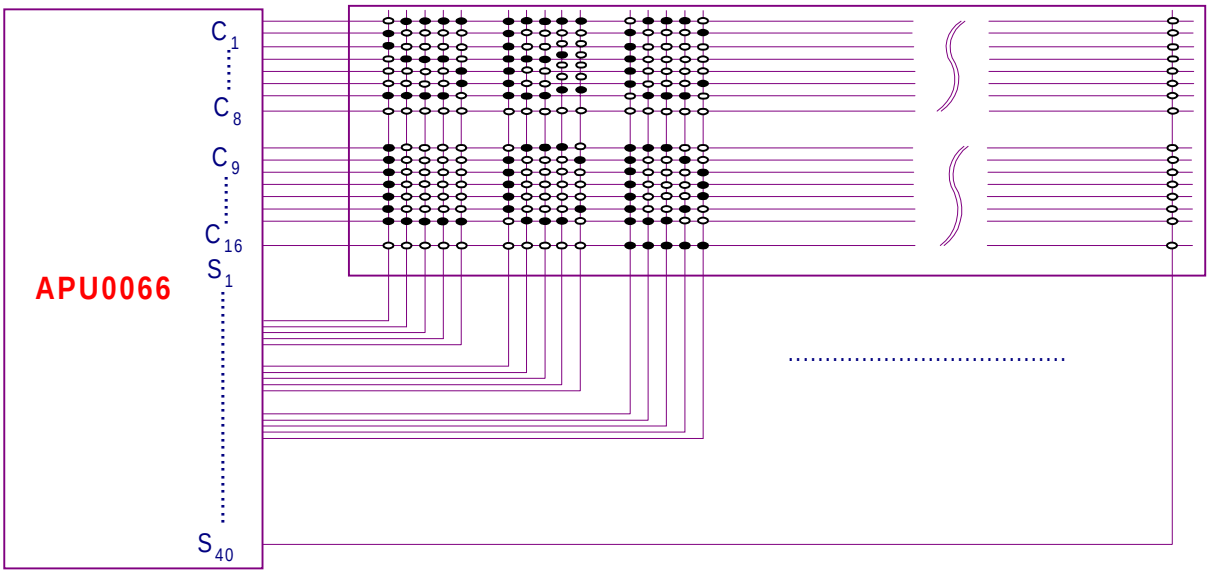
1. LCD Panel : 8 character × 1 line character format ; 5 × 7 dots + 1 cursor line (1/4 bias, 1/8 duty)



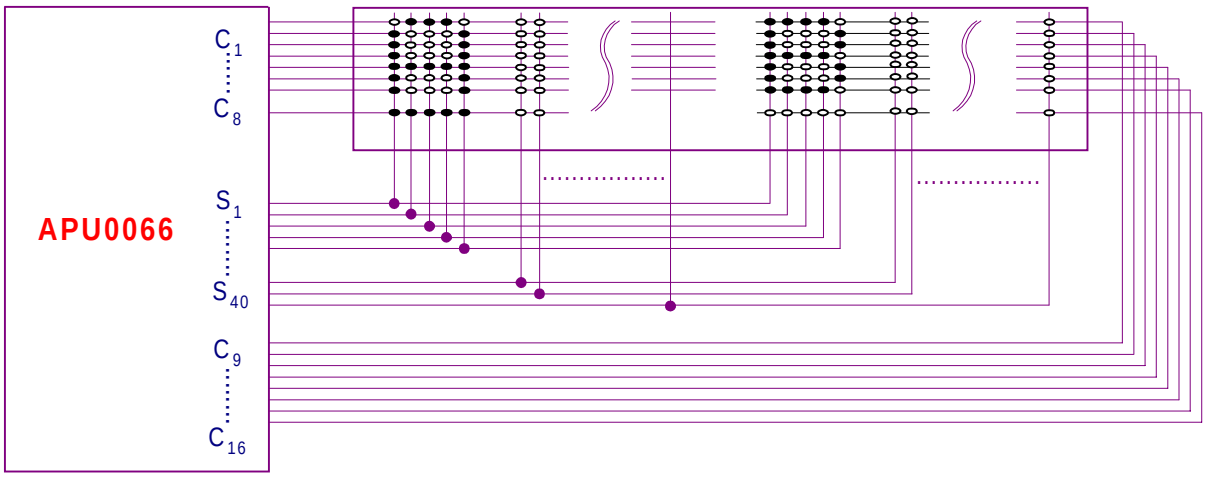
2. LCD Panel : 8 character × 1 line character format ; 5 × 10 dots + 1 cursor line (1/4 bias, 1/8 duty)



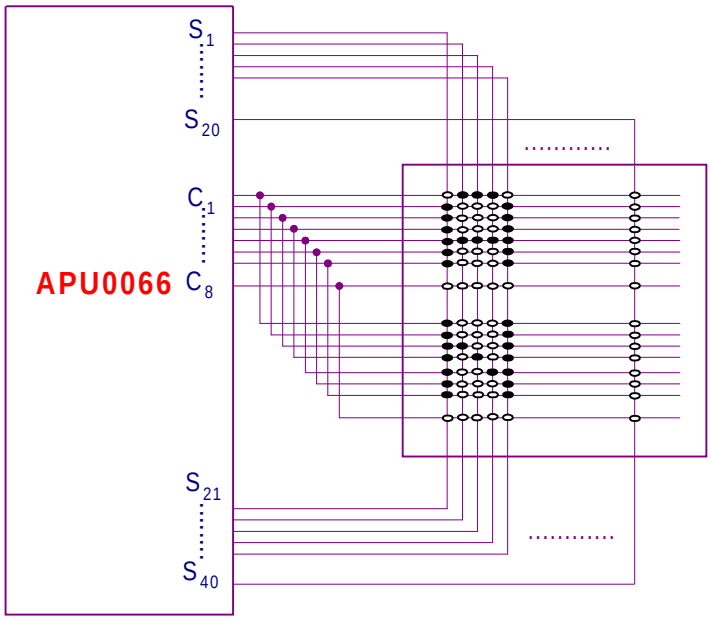
3. LCD Panel : 8 character × 2 line character format ; 5 × 7 dots + 1 cursor line (1/5 bias, 1/16 duty)



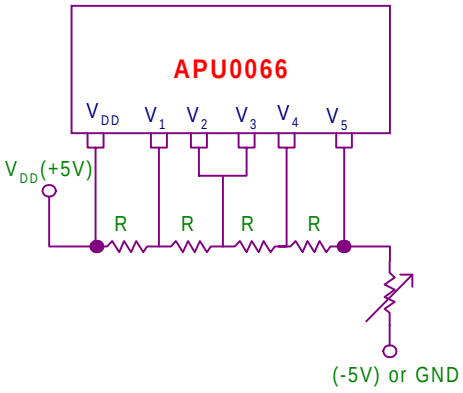
4. LCD Panel : 16 character × 1 line character format ; 5 × 7 dots + 1 cursor line (1/5 bias, 1/16 duty)

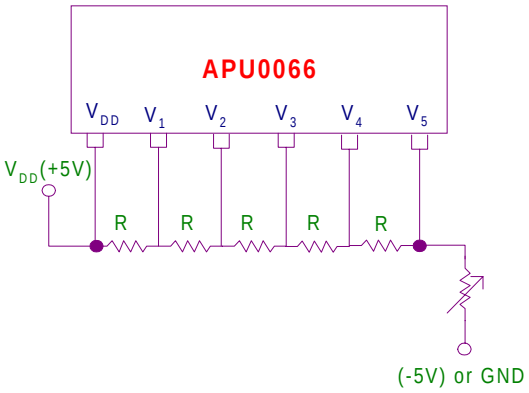


5. LCD Panel : 4 character × 2 line character format ; 5 × 7 dots + 1 cursor line (1/4 bias, 1/8 duty)



BIAS VOLTAGE DIVIDE CIRCUIT





STANDARD CHARACTER PATTERN